ANALOG DEVICES

Digital PAL/NTSC Video Encoder with 10-Bit SSAF™ & Advanced Power Management

Preliminary Technical Information

ADV7170/ADV7171

FEATURES

- ITU-R BT601/656 YCrCb to PAL/NTSC Video Encoder
- High Quality 10-Bit Video DACs
- SSAF™ (Super Sub-Alias Filter)
- Advanced Power Management features
- CGMS (Copy Generation Management System)
- WSS (Wide Screen Signalling)
- Simultaneous Y, U, V, C Output Format
- NTSC-M, PAL-M, PAL-B/D/G/H/I
- Single 27MHz Clock Required (x2 oversampling)
- 80 dB Video SNR
- 32-Bit Direct Digital Synthesiser for Color Sub-Carrier
- Multi-standard video output support:
  - Composite (CVBS)
  - Component S-Video (Y/C)
  - Component YUV & RGB
  - EuroSCART Output (RGB + CVBS/LUMA)
  - Component YUV + CHROMA
- Video Input Data Port supports:
  - CCIR-656 4:2:2 8-Bit Parallel Input Format
  - 4:2:2 16-Bit Parallel Input Format
- SMPTE 170M NTSC Compatible Composite Video
- ITU-R BT.470 PAL Compatible Composite Video
- Programmable Simultaneous Composite and S-VHS Y/C or RGB(SCART)/YUV Video Outputs.
- Programmable Luma Filters (Low-Pass(PAL/NTSC), Notch, Extended(SSAF), CIF and QCIF)
- Programmable Chroma Filters (Low-Pass(0.65MHz, 1.0MHz, 1.2MHz and 2.0MHz), CIF and QCIF)
- Programmable VBI (Vertical Blanking Interval)
- Programmable Sub-Carrier Frequency and Phase.
- Programmable LUMA Delay
- Individual ON/OFF Control of Each DAC
- CCIR & Square Pixel Operation
- Integrated Subcarrier Locking to external Video Source
- Color Signal Control/Burst Signal Control
- Interlaced/Non Interlaced Operation
- Complete on-chip Video Timing Generator
- Programmable Multi-Mode Master/Slave Operation
- Macrovision Anti-Taping Rev 7.1 (ADV7170 only)*
- Close Captioning support.
- Teletext Insertion Port (PAL-WST)
- On Board Color Bar Generation
- On Board Voltage Reference
- 2 Wire Serial MPU Interface (I^2C Compatible & Fast I^2C)
- Single Supply +5 V or + 3.3V Operation
- Small 44-Pin PQFP Thermally Enhanced Package

APPLICATIONS

High Performance DVD Playback Systems, Portable Video Equipment including Digital Still Cameras and Laptop PCs

GENERAL DESCRIPTION

The ADV7170/ADV7171 is an integrated Digital Video Encoder that converts Digital CCIR-601 4:2:2 8 or 16-bit Component Video Data into a standard analog baseband television signal compatible with world wide standards.

The on-board SSAF™ (Super Sub-Alias Filter), with extended luminance frequency response and sharp stop-band attenuation enables studio quality video playback on modern TVs giving optimal horizontal line resolution.

An advanced power managment circuit enables optimal control of power consumption in both normal operating modes and power down or sleep modes.

The ADV7170/ADV7171 also supports both PAL and NTSC square pixel operation. The parts also incorprate WSS and CGMS-A data control generation.

The Output Video Frames are synchronised with the incoming data Timing Reference Codes. Optionally the Encoder accepts (and can generate) $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ & FIELD Timing Signals. These timing signals can be adjusted to change pulse width and position while the part is in the master mode. The Encoder requires a single two times pixel rate (27 MHz) Clock for standard operation. Alternatively the Encoder requires a 24.54 MHz Clock for NTSC or 29.5MHz Clock for PAL square pixel mode operation. All internal timing is generated on-chip.

A separate teletext port enables the user to directly input teletext data during the vertical blanking interval.

The ADV7170/ADV7171 modes are set up over a two wire serial bi-directional port (I^2C Compatible) with 2 slave addresses.

Functionally the ADV7171 and ADV7170 are the same with the exception that the ADV7170 can output the Macrovision* anticopy algorithm.

The ADV7170/ADV7171 is packaged in a 44-Pin thermally enhanced PQFP package (Patent pending).

The ADV7170/ADV7171 is protected by US patents numbers 5,343,196 and 5,442,355 and other intellectual property rights.

Note: ITU-R and CCIR are used interchangably in this document (ITU-R has replaced CCIR recommendations).

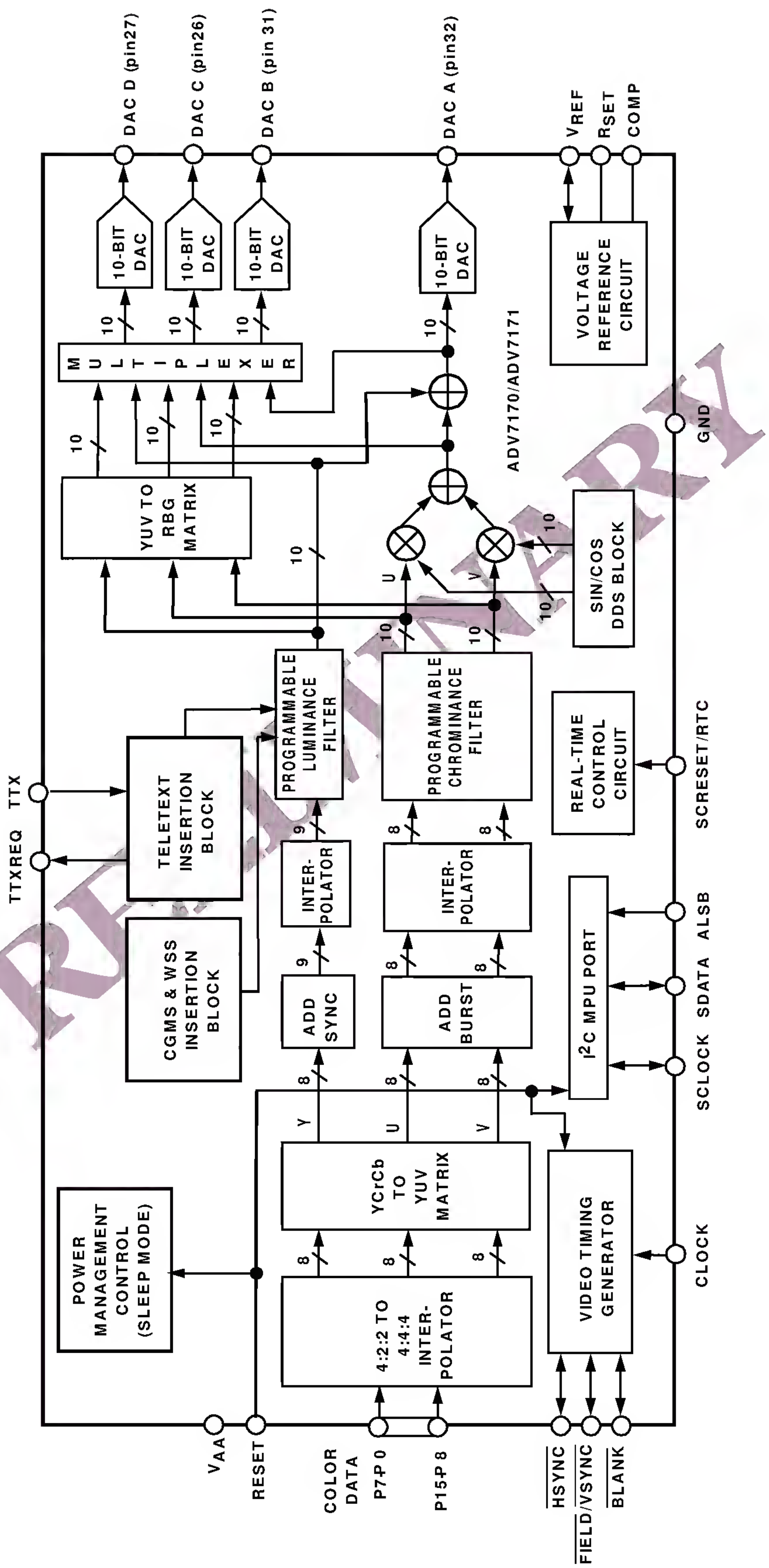
SSAF™ is a trademark of Analog Devices, Inc.

* This device is protected by U.S. patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. The Macrovision anticopy process is licensed for non-commercial home use only, which is its sole intended use in the device. Please contact sales office for latest Macrovision version available.

Oct 97 REV. 01

One Technology Way, P.O. Box 9106, Norwood. MA 02062-9106, U.S.A.
Tel: 617/329-4700 World Wide Web Site: http://www.analog.com
Fax: 617/326-8703

FUNCTIONAL BLOCK DIAGRAM



5V SPECIFICATIONS (V_{AA} = + 5V ± 5%[1], V_{REF} = 1.235 V R_{SET} = 150 Ω All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions[1]
STATIC PERFORMANCE					
Resolution (each DAC)			10	Bits	
Accuracy (each DAC)					
Integral Nonlinearity			±1	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}[3]			±1	μA	V_{IN} = 0.4 V or 2.4 V
Input Current, I_{IN}[4]			±50	μA	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}		10		pF	
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 3.2 mA
Tri-State Leakage Current			10	μA	
Tri-State Output Capacitance		10		pF	
ANALOG OUTPUTS					
Output Current[5]	16.5	17.4	18.5	mA	
Output Current[6]		5		mA	
DAC to DAC Matching		0.6	5	%	
Output Compliance, V_{OC}	0		+1.4	V	
Output Impedance, R_{OUT}		15		KΩ	
Output Capacitance, C_{OUT}			30	pF	I_{OUT} = 0 mA
VOLTAGE REFERENCE					
Reference Range, V_{REF}	1.112	1.235	1.359	V	$I_{VREFOUT}$ = 20 μA
POWER REQUIREMENTS[7]					
V_{AA}	4.75	5.0	5.25	V	
Normal Power Mode					
I_{DAC}(max)[8]		150	155	mA	
I_{DAC}(min)[8]		20		mA	
I_{CCT}[9]		65		mA	
Low Power Mode					
I_{DAC}(max)[8]		80		mA	
I_{DAC}(min)[8]		15		mA	
I_{CCT}[9]		65		mA	
Sleep Mode					
I_{DAC}[10]		10		μA	
I_{CCT}[11]		10		μA	
Power Supply Rejection Ratio		0.01	0.5	% / %	COMP = 0.1μF

NOTES

[1] The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V range
[2] Temperature Range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3] All digital input pins except pins $\overline{\text{RESET}}$ and RTC/SCRESET.
[4] Excluding all digital input pins except pins $\overline{\text{RESET}}$ and RTC/SCRESET.
[5] Full drive into 75 Ohm load.
[6] Minimum drive current (used with buffered/scaled output load).
[7] Power measurements are taken with Clock Frequency = 27 MHz. Max T_J = 110°C.
[8] I_{DAC} is the total current *("min" corresponds to 5 mA output per DAC, "max" corresponds to 38 mA output per DAC)* to drive all 4 DACs. Turning off individual DACs reduces I_{DAC} correspondingly.
[9] I_{CCT} (Circuit Current) is the continuous current required to drive the device.
[10] Total DAC current in Sleep mode.
[11] Total continuous current during Sleep mode.
Specifications subject to change without notice.

3.3V SPECIFICATIONS

(V_{AA} = + 3.0V - 3.6V[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω
All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions[1]
STATIC PERFORMANCE[10]					
Resolution (each DAC)			10	Bits	
Accuracy (each DAC)					
Integral Nonlinearity		±1		LSB	
Differential Nonlinearity		±1		LSB	Guaranteed Monotonic
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2		V	
Input Low Voltage, V_{INL}		0.8		V	
Input Current, I_{IN}[3,10]			±1	µA	V_{IN} = 0.4 V or 2.4 V
Input Current, I_{IN}[4,10]			±50	µA	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}		10		pF	
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}		2.4		V	I_{SOURCE} = 400 µA
Output Low Voltage, V_{OL}		0.4		V	I_{SINK} = 3.2 mA
Tri-State Leakage Current[10]			10	µA	
Tri-State Output Capacitance[10]		10		pF	
ANALOG OUTPUTS[10]					
Output Current[5,11]	33	34.7	37	mA	R_{set} = 150Ω, RL= 75Ω
Output Current[6]		5		mA	
DAC to DAC Matching		2.0		%	
Output Compliance, V_{OC}	0		+1.4	V	
Output Impedance, R_{OUT}		15		KΩ	
Output Capacitance, C_{OUT}			30	pF	I_{OUT} = 0 mA
POWER REQUIREMENTS[7,10]					
V_{AA}	3.0	3.3	3.6	V	
Normal Power Mode					
I_{DAC}(max)[8]		150	155	mA	R_{set} = 300Ω, RL = 150Ω
I_{DAC}(min)[8]		20		mA	
I_{CCT}[9]		30		mA	
Low Power Mode					
I_{DAC}(max)[8]		75		mA	
I_{DAC}(min)[8]		15		mA	
I_{CCT}[9]		30		mA	
Sleep Mode					
I_{DAC}[12]		10		µA	
I_{CCT}[13]		10		µA	
Power Supply Rejection Ratio		0.01	0.5	% / %	COMP = 0.1µF

NOTES

[1] The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V range

[2] Temperature Range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3] All digital input pins except pins $\overline{\text{RESET}}$ and RTC/SCRESET .

[4] Excluding all digital input pins except pins $\overline{\text{RESET}}$ and RTC/SCRESET.

[5] Full drive into 37.5 Ohm load.

[6] Minimum drive current (used with buffered/scaled output load).

[7] Power measurements are taken with Clock Frequency = 27 MHz. Max T_J = 110°C.

[8] I_{DAC} is the total current *("min" corresponds to 5 mA output per DAC, "max" corresponds to 38 mA output per DAC)* to drive all 4 DACs. Turning off individual DACs reduces I_{DAC} correspondingly.

[9] I_{CCT} (Circuit Current) is the continuous current required to drive the device.

[10] Guaranteed by Characterisation.

[11] DAC's can output 35mA typically at 3.3V (Rset = 150Ω and RL =75), optimum performance obtained at 18mA DAC current (Rset = 300Ω and RL =150Ω).

[12] Total DAC current in Sleep mode.

[13] Total continuous current during Sleep mode.

Specifications subject to change without notice.

5V DYNAMIC-SPECIFICATIONS[1]

(V_{AA} = + 4.75V - 5.25 V [1], V_{REF} = 1.235 V R_{SET} =150 Ohms
All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Conditions[1]
Differential Gain[4]		0.7		%	Normal Power Mode
Differential Phase[4]		0.7		°	Normal Power Mode
Differential Gain[4]		2.0		%	Lower Power Mode
Differential Phase[4]		1.0		°	Lower Power Mode
SNR[4] (Pedestal)		80		dB rms	RMS
SNR[4] (Pedestal)		70		dB p-p	Peak Periodic
SNR[4] (Ramp)		60		dB rms	RMS
SNR[4] (Ramp)		58		dB p-p	Peak Periodic
Hue Accuracy[4]		0.8		°	
Color Saturation Accuracy[4]		1.0		%	
Chroma Nonlinear Gain[4]		0.6		± %	Referenced to 40 IRE
Chroma Nonlinear Phase[4]		0.6		± °	NTSC
Chroma Nonlinear Phase[4]		0.4		± °	PAL
Chroma/Luma Intermod[4]		0.3		± %	Referenced to 714 mV (NTSC)
Chroma/Luma Intermod[4]		0.3		± %	Referenced to 700 mV (PAL)
Chroma/Luma Gain Ineq[4]		0.6		± %	
Chroma/Luma Delay Ineq[4]		2.0		ns	
Luminance Nonlinearity[4]		1.0		± %	
Chroma AM Noise[4]		66		dB	
Chroma PM Noise[4]		63		dB	

NOTES
1 Temperature Range T_{MIN} to T_{MAX}: 0°C to 70°C.
2 Characterised by Design.
3 These specifications are for the low pass filter only and guaranteed by design. For the other internal filters please see Figure 3.
4 Guaranteed by characterisation.

Specifications subject to change without notice.

3.3V DYNAMIC-SPECIFICATIONS

(V_{AA} = + 4.75V - 5.25 V [1], V_{REF} = 1.235 V R_{SET} = 150 Ohms All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Conditions[1]
Differential Gain[4]		TBD		%	Normal Power Mode
Differential Phase[4]		TBD		°	Normal Power Mode
Differential Gain[4]		TBD		%	Lower Power Mode
Differential Phase[4]		TBD		°	Lower Power Mode
SNR[4] (Pedestal)		78		dB rms	RMS
SNR[4] (Pedestal)		70		dB p-p	Peak Periodic
SNR[4] (Ramp)		60		dB rms	RMS
SNR[4] (Ramp)		58		dB p-p	Peak Periodic
Hue Accuracy[4]		TBD		°	
Color Saturation Accuracy[4]		TBD		%	
Luminance Nonlinearity[4]		TBD		±%	
Chroma AM Noise[4]		TBD		dB	
Chroma PM Noise[4]		TBD		dB	

NOTES

[1] Temperature Range T_{MIN} to T_{MAX}: 0°C to 70°C.
[2] Characterised by Design.
[3] These specifications are for the low pass filter only and guaranteed by design. For the other internal filters please see Figure 3.
[4] Guaranteed by characterisation.

Specifications subject to change without notice.

5V TIMING–SPECIFICATIONS

(V_{AA} = 4.75 - 5.25 [1], V_{REF} = 1.235 V R_{SET} = 150 Ohms All specifications T_{MIN} to T_{MAX} [2] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Condition
MPU PORT[4]					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulse Width, t_1	0.6			µs	
SCLOCK Low Pulse Width, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After this period the 1st clock is generated
Setup Time (Start Condition), t_4	0.6			µs	Relevent for repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition) , t_8	0.6			µs	
ANALOG OUTPUTS[4,5]					
Analog Output Delay		5		ns	
DAC Analog Output Skew		0		ns	
CLOCK CONTROL AND PIXEL PORT[3,4,6]					
F_{CLOCK}		27		MHz	
Clock High Time t_9	8			ns	
Clock Low Time t_{10}	8			ns	
Data Setup Time t_{11}	3.5			ns	
Data Hold Time t_{12}	4			ns	
Control Setup Time t_{11}	4			ns	
Control Hold Time t_{12}	3			ns	
Digital Output Access Time t_{13}			24	ns	
Digital Output Hold Time t_{14}		4		ns	
Pipeline Delay t_{15}		37		Clock cycles	
TELETEXT PORT[3,4,7]					
Digital Output Acces Time t_{16}		20		ns	
Data Setup Time t_{17}		1		ns	
Data Hold Time t_{18}		2		ns	
RESET CONTROL[3,4,8]					
Reset Low Time	6			ns	

NOTES

[1] The max/min specifications are guaranteed over this range.
[2] Temperature Range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3] Characterised by Design
[4] TTL input values are 0 to 3 volts, with input rise/fall times - 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load - 10 pF.
[5] Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.
[6] Pixel Port consists of the following:

Pixel Inputs:	P15-P0
Pixel Controls:	$\overline{HSYNC}$, FIELD/$\overline{VSYNC}$, $\overline{BLANK}$
Clock Input:	CLOCK

[7] Teletext Port consists of the following:

Teletext Output:	TTXREQ
Teletext Input:	TTX

[8] Guaranteed by characterisation.

Specifications subject to change without notice.

3.3V TIMING–SPECIFICATIONS (V_{AA} = 3.0 - 3.6 [1], V_{REF} = 1.235 V R_{SET} = 150 Ohms All specifications T_{MIN} to T_{MAX} [2] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Condition
MPU PORT[4,8]					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulse Width, t_1	0.6			µs	
SCLOCK Low Pulse Width, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After this period the 1st clock is generated
Setup Time (Start Condition), t_4	0.6			µs	Relevent for repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition) , t_8	0.6			µs	
ANALOG OUTPUTS[4,5]					
Analog Output Delay		7		ns	
DAC Analog Output Skew		0		ns	
CLOCK CONTROL AND PIXEL PORT[3,4,6,8]					
F_{CLOCK}		27		MHz	
Clock High Time t_9	8			ns	
Clock Low Time t_{10}	8			ns	
Data Setup Time t_{11}	3.5			ns	
Data Hold Time t_{12}	4			ns	
Control Setup Time t_{11}	4			ns	
Control Hold Time t_{12}	3			ns	
Digital Output Access Time t_{13}			24	ns	
Digital Output Hold Time t_{14}		4		ns	
Pipeline Delay t_{15}		37		Clock cycles	
TELETEXT PORT[3,4,7]					
Digital Output Acces Time t_{16}		23		ns	
Data Setup Time t_{17}		2		ns	
Data Hold Time t_{18}		2		ns	
RESET CONTROL[3,4,8]					
Reset Low Time	6			ns	

NOTES

[1] The max/min specifications are guaranteed over this range.

[2] Temperature Range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3] Characterised by Design

[4] TTL input values are 0 to 3 volts, with input rise/fall times - 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load - 10 pF.

[5] Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

[6] Pixel Port consists of the following:

Pixel Inputs:	P15-P0
Pixel Controls:	$\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
Clock Input:	CLOCK

[7] Teletext Port consists of the following:

Teletext Output:	TTXREQ
Teletext Input:	TTX

[8] Guaranteed by characterisation.

Specifications subject to change without notice.

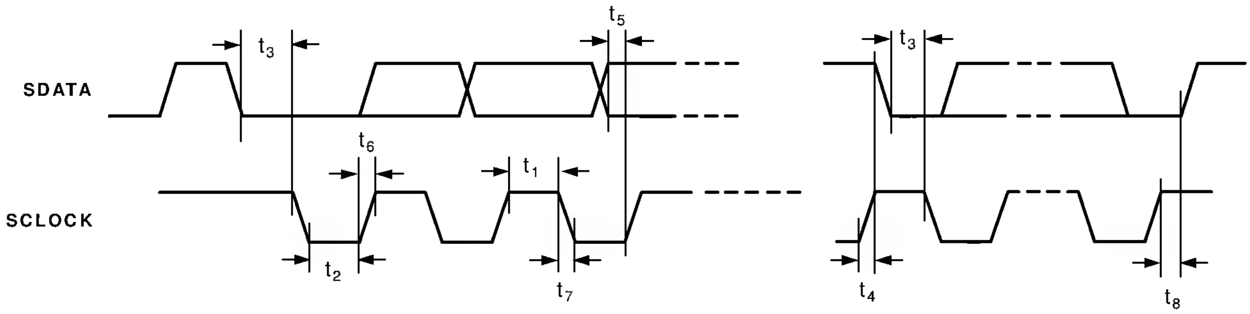


Figure 0. MPU Port Timing Diagram

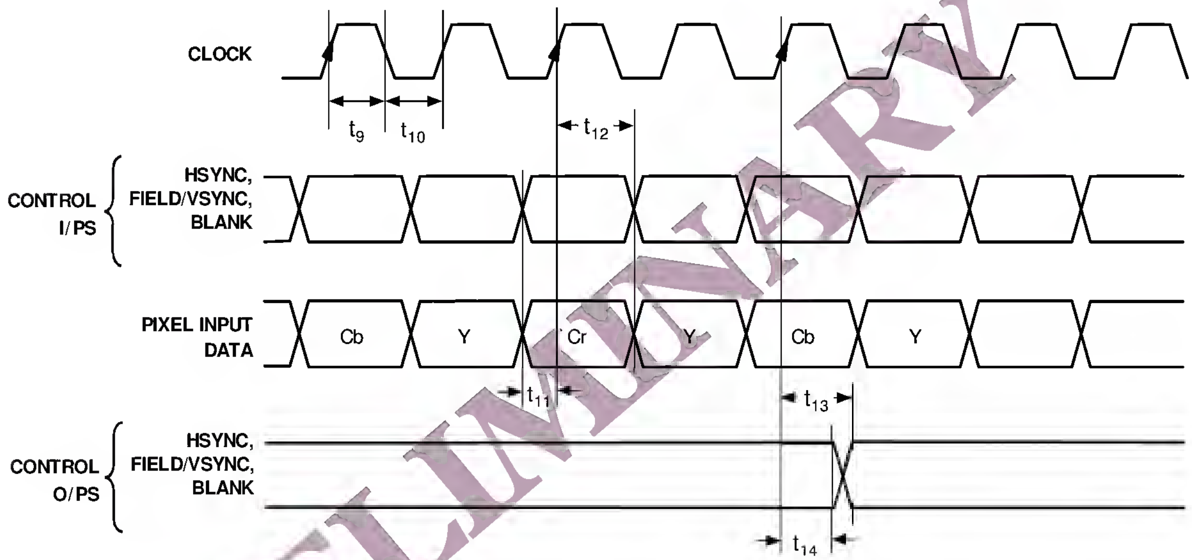


Figure 1. Pixel and Control Data Timing Diagram

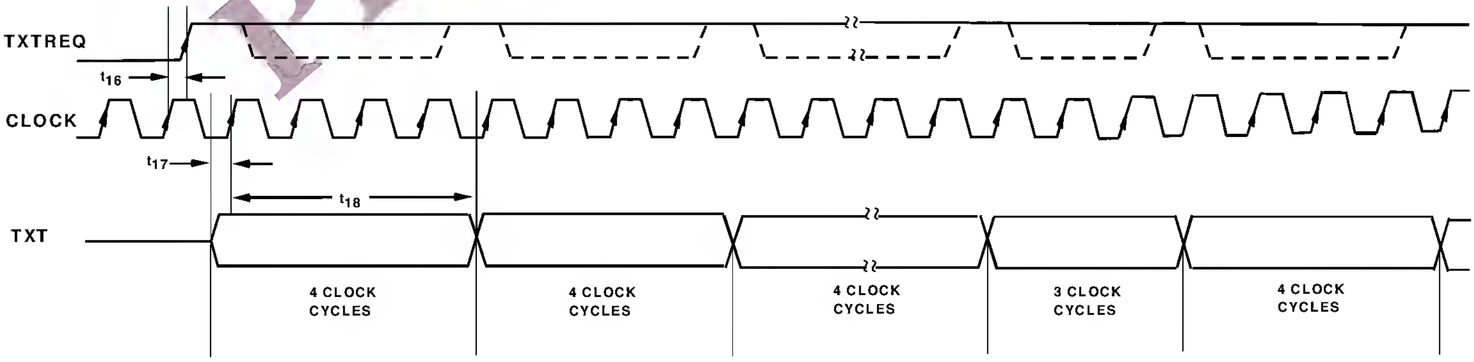


Figure 2. Teletext Timing Diagram

ABSOLUTE MAXIMUM RATINGS *

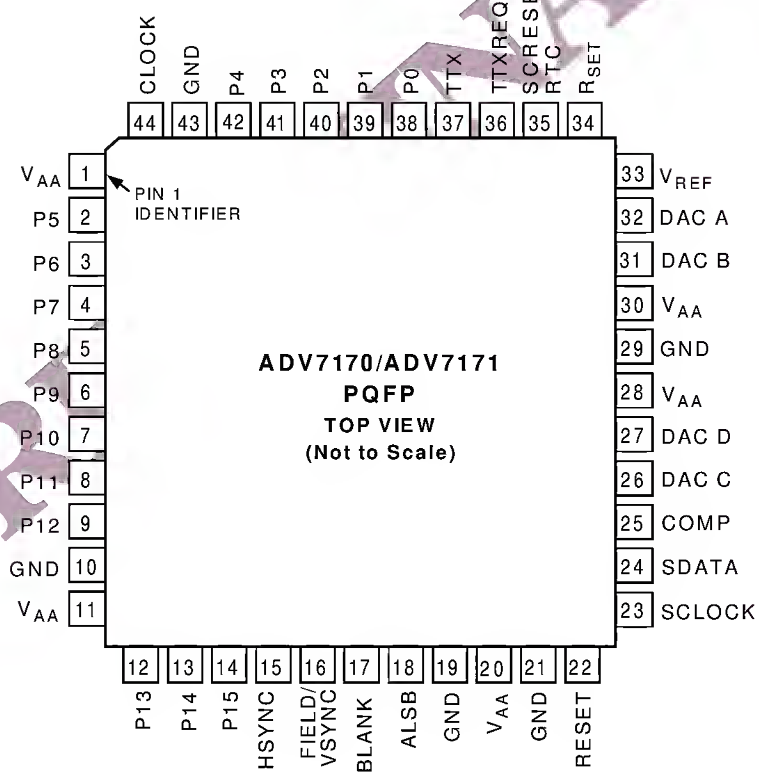
V_{AA} to GND 7V
Voltage on any Digital Input Pin ....GND-0.5V to V_{AA}+0.5V
Storage Temperature (T_S) ....-65°C to +150°C
Junction Temperature(T_J) ....+150°C
Lead Temperature (Soldering, 10 secs) ....+260°C
Analog Outputs to GND[1] ....GND -0.5 to V_{AA}

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

ORDERING GUIDE

Model Option	Temperature Range	Package
ADV7175AKS	0°C to 70°C	S-44
ADV7176AKS	0°C to 70°C	S-44

PIN CONFIGURATION



CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7170/ADV7171 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESCRIPTION

Mnemonic	Input/Output	Function
P15-P0	I	8-Bit 4:2:2 Multiplexed YCrCb Pixel Port (P7-P0) or 16-Bit YCrCb Pixel Port (P15-P0). P0 represents the LSB.
CLOCK	I	TTL Clock Input. Requires a stable 27MHz reference Clock for standard operation. Alternatively a 24.52MHz (NTSC) or 29.5MHz (PAL) can be used for square pixel operation.
$\overline{\text{HSYNC}}$	I/O	$\overline{\text{HSYNC}}$ (Modes 1 &2) Control Signal. This pin may be configured to output (Master Mode) or accept (Slave Mode) Sync signals.
FIELD / $\overline{\text{VSYNC}}$	I/O	Dual Function FIELD (Mode 1) and $\overline{\text{VSYNC}}$ (Mode 2) Control Signal. This pin may be configured to output (Master Mode) or accept (Slave Mode) these control signals.
$\overline{\text{BLANK}}$	I/O	Video Blanking Control Signal. The pixel inputs are ignored when this is logic level "0". This signal is optional.
SCRESET /RTC	I	This pin can be configured as an input by setting MR22 and MR21 of Mode Register 2. It can be configured as a subcarrier reset pin, in which case a high to low transition on this pin will reset the subcarrier to field 0. Alternatively it may be configured as a Real Time Control(RTC) input.
V_{REF}	I/O	Voltage Reference Input for DACs or Voltage Reference Output (1.235V).
R_{SET}	I	A 150 Ohm resistor connected from this pin to GND is used to control full-scale amplitudes of the Video Signals.
COMP	O	Compensation Pin. Connect a 0. 1μF Capacitor from COMP to V_{AA}. For Optimum Dynamic Performance in Low Power Mode, the value of the COMP capacitor can be lowered to as low as 2.2nF.
DAC A	O	PAL/NTSC Composite Video Output. Full-Scale Output is 180IRE (1286mV) for NTSC and 1300mV for PAL.
DAC C	O	RED / S-VHS C / V Analog Output.
DAC D	O	GREEN / S-VHS Y / Y Analog Output
DAC B	O	BLUE / Composite / U Analog Output.
SCLOCK	I	MPU Port Serial Interface Clock Input.
SDATA	I/O	MPU Port Serial Data Input/Output.
ALSB	I	TTL Address Input. This signal set up the LSB of the MPU address.
$\overline{\text{RESET}}$	I	The input resets the on chip timing generator and sets the ADV7170/ ADV7171 into default mode. This is NTSC operation, Timing Slave Mode 0, 8 Bit Operation, 2 x Composite & S VHS out and all DAC"s powered ON
TTX / V_{AA}	I	Teletetext Data / Defaults to V_{AA} when Teletext not Selected (enables backward compatibility to ADV7175/ADV7176
TTRQEQ / GND	O	Teletext Data Request Signal / Defaults to GND when Teletext not Selected (enables backward compatibility to ADV7175/ADV7176
V_{AA}	P	Power Supply (+3 V to + 5 V).
GND	G	Ground Pin.

DATA PATH DESCRIPTION.

For PAL B,D,G,H,I,M,N and NTSC M,N modes, YCrCb 4:2:2 Data is input via the CCIR-656 Compatible Pixel Port at a 27MHz Data Rate. The Pixel Data is demultiplexed to form three data paths. Y has typically a range of 16 to 235, Cr and Cb have typically a range of 128+/-112, however it is possible to input data form 1 to 254 on both Y,Cb and Cr. The ADV7170/ADV7171 supports PAL (B,D,G,H,I,N,M) and NTSC (with and without Pedestal) standards. The appropriate SYNC, BLANK and Burst levels are added to the YCrCb data. Macrovision Anti-Taping (ADV7170 only), Closed-Captioning and Teletext levels are also added to Y and the resultant data is interpolated to a rate of 27MHz. The interpolated data is filtered and scaled by three Digital FIR Filters.

The U and V Signals are modulated by the appropriate Sub-Carrier Sine/Cosine Phases and added together to make up the Chrominance Signal. The Luma (Y) signal can be delayed 1-3 Luma Cycles (each cycle is 74ns) with respect to the Chroma Signal. The Luma and Chroma signals are then added together to make up the Composite Video Signal. All edges are slew rate limited.

The YCrCb Data is also used to generate RGB data with appropriate SYNC and BLANK Levels. The RGB data is in sychronisation with the composite video output. Alternatively analog YUV data can be generated instead of RGB.

The four 10-Bit DACs can be used to output :-

(1) Composite Video + RGB Video

(2) Composite Video + YUV Video

(3) Two Composite Video Signals
+ LUMA & CHROMA (Y/C) Signals.

Alternatively, each DAC can be individually powered off if not required.

Video output levels are illustrated in Appendix 3, 4 and 5.

INTERNAL FILTER RESPONSE

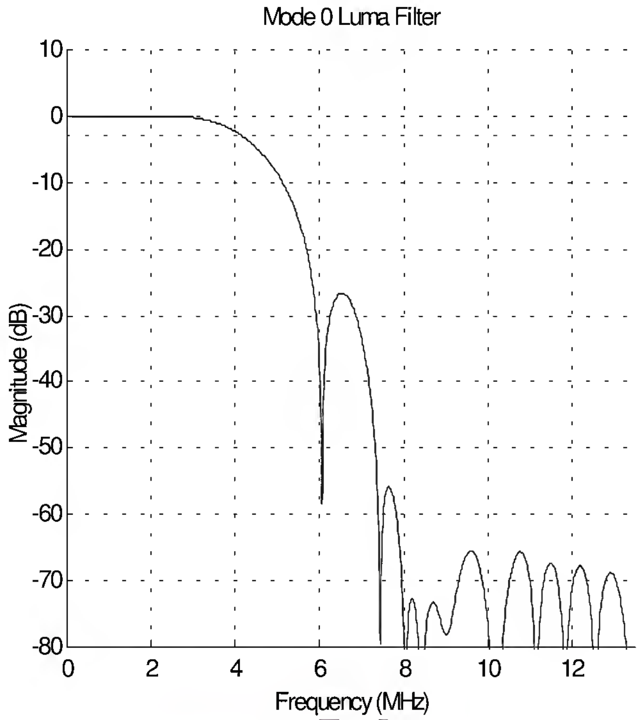
The Y Filter supports several different frequency responses including two Low Pass responses, two notch responses, an Extended (SSAF) response , a CIF response and a QCIF response. The UV Filter supports several different frequency responses including four Low Pass responses, a CIF response and a QCIF response, these can be seen in the following Figures 3 to 11.

FILTER TYPE	FILTER SELECTION			PASSBAND RIPPLE (dB)	3dB BANWIDTH (MHz)	STOPBAND CUTOFF(MHz)	STOPBAND ATTENUATION(dB)
	MR04	MR03	MR02				
LOW PASS (NTSC)	0	0	0	0.091	4.157	7.37	-56
LOW PASS (PAL)	0	0	1	0.15	4.74	7.96	-64
NOTCH (NTSC)	0	1	0	0.015	6.54	8.3	-68
NOTCH (PAL)	0	1	1	0.095	6.24	8.0	-66
EXTENDED (SSAF)	1	0	0	0.051	6.217	8.0	-61
CIF	1	0	1	0.018	3.0	7.06	-61
QCIF	1	1	0	Monotonic	1.5	7.15	-50

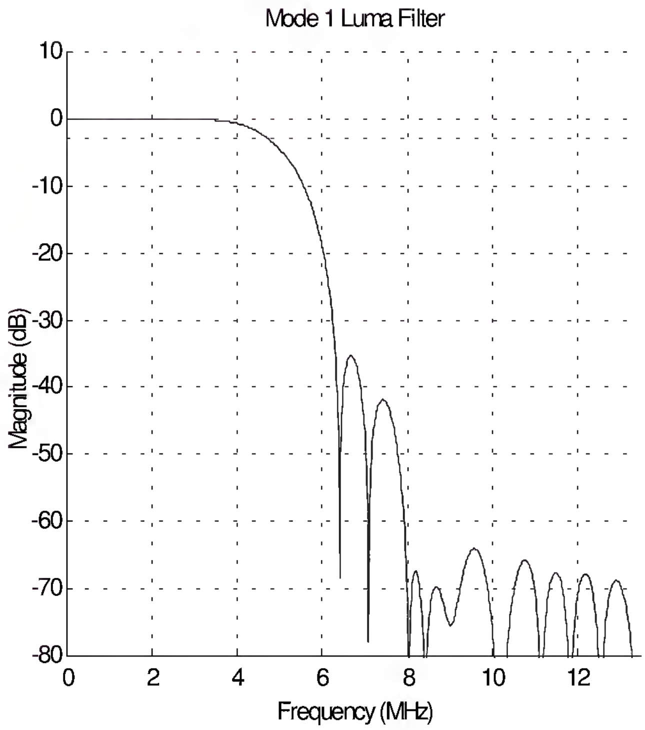
Figure 3. Luminance Internal Filter Specifications

FILTER TYPE	FILTER SELECTION			PASSBAND RIPPLE (dB)	3dB BANWIDTH (MHz)	STOPBAND CUTOFF(MHz)	STOPBAND ATTENUATION(dB)
	MR07	MR06	MR05				
1.3MHzLOW PASS	0	0	0	0.084	1.395	3.01	-45
0.65MHzLOW PASS	0	0	1	Monotonic	0.65	3.64	-58.5
1.0MHz LOW PASS	0	1	0	Monotonic	1.0	3.73	-49
2.0MHz LOW PASS	0	1	1	0.0645	2.2	5.0	-40
RESERVED	1	0	0				
CIF	1	0	1	0.084	1.395	3.01	-45
QCIF	1	1	0	Monotonic	0.5	4.08	-50

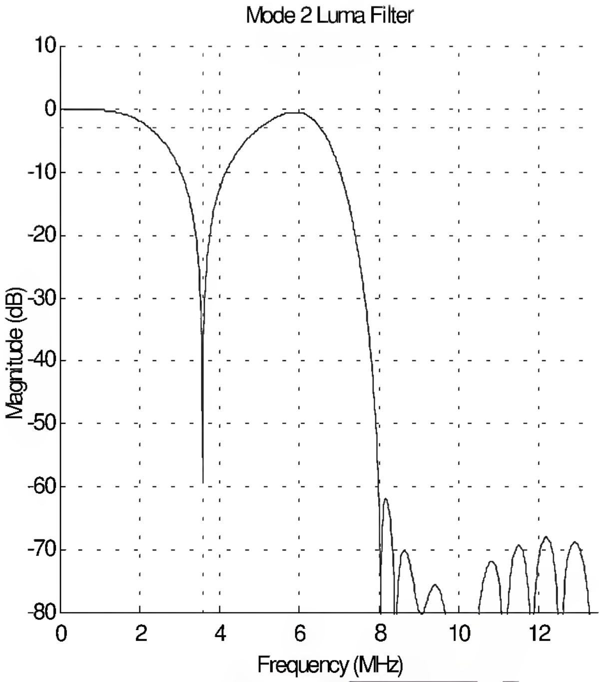
Figure 4. Chrominance Internal Filter Specifications



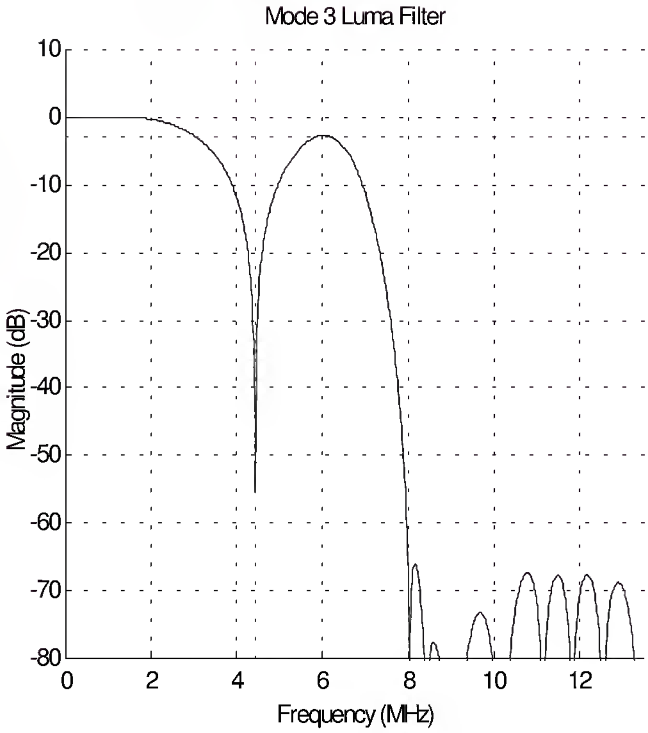
NTSC Low Pass Luma Filter



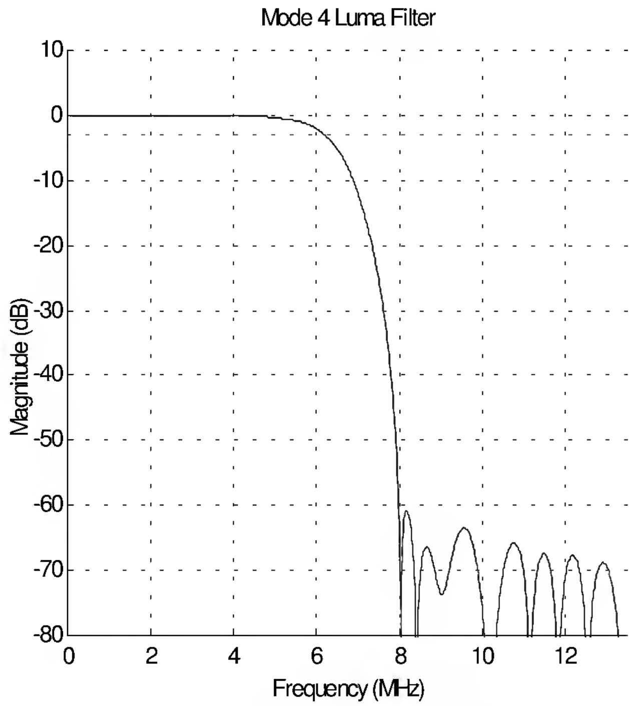
PAL Low Pass Luma Filter



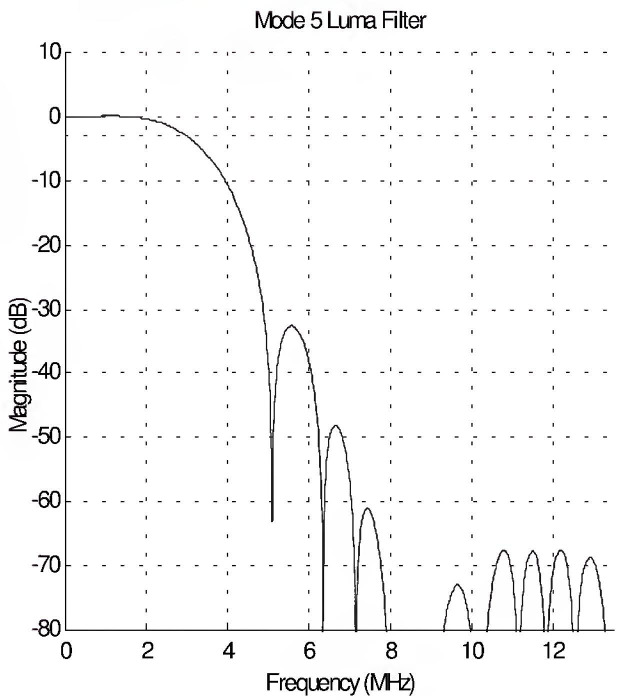
NTSC Notch Luma Filter



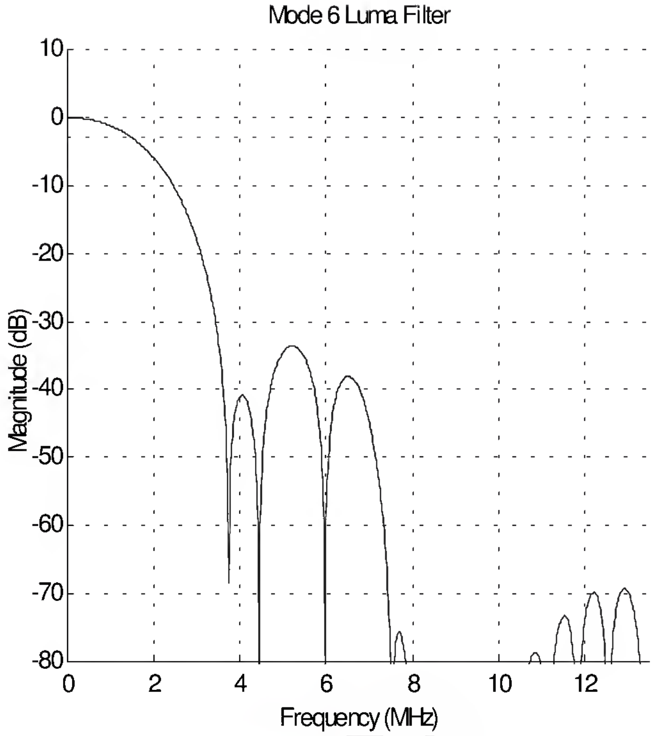
PAL Notch Luma Filter



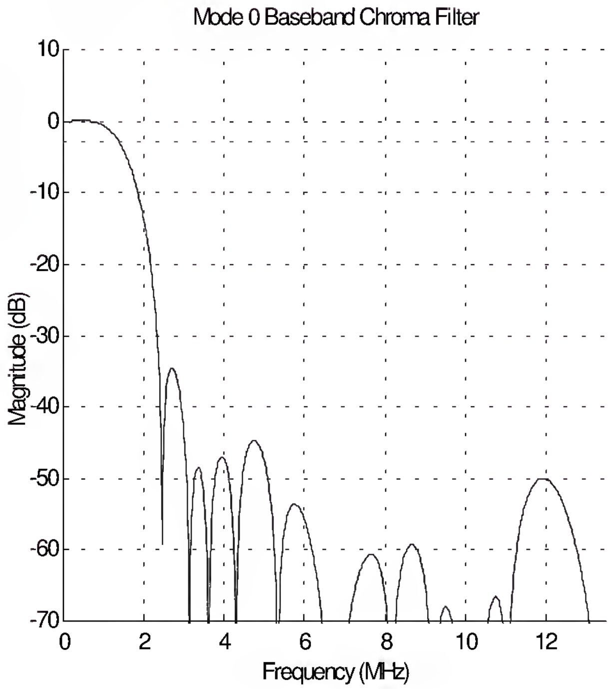
Extended Mode (SSAF) Luma Filter



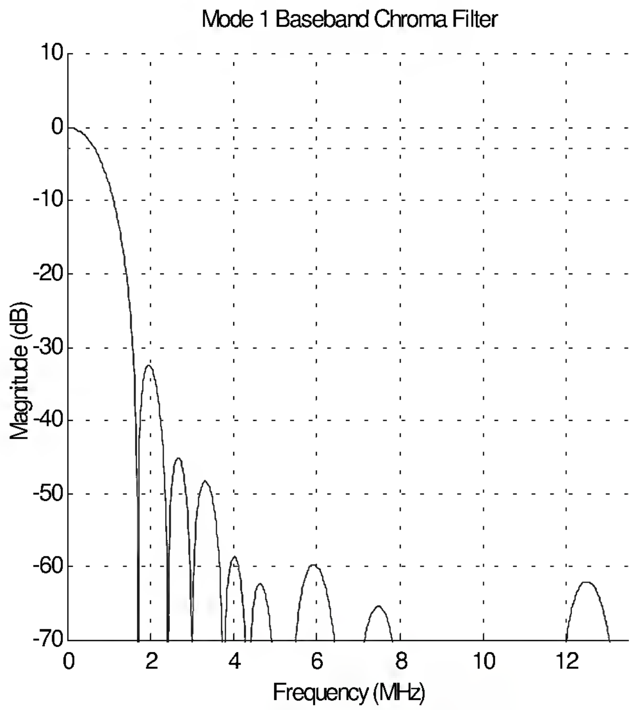
CIF Luma Filter



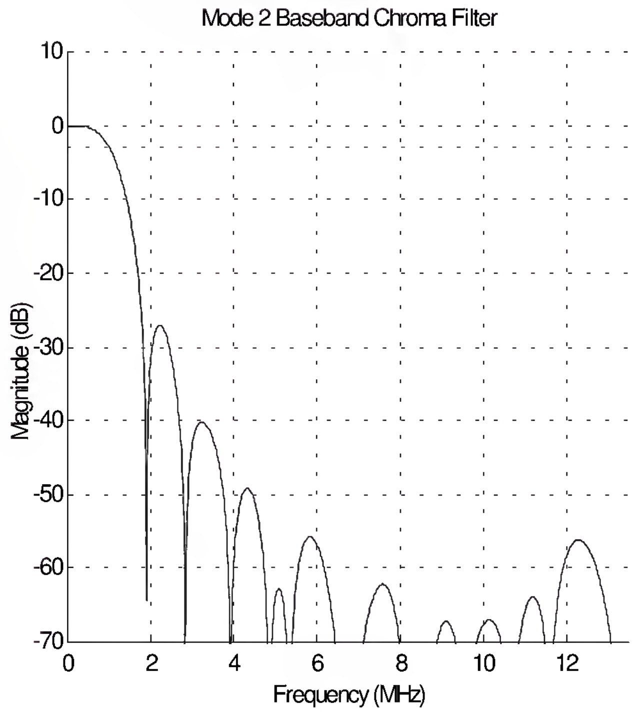
QCIF Luma Filter



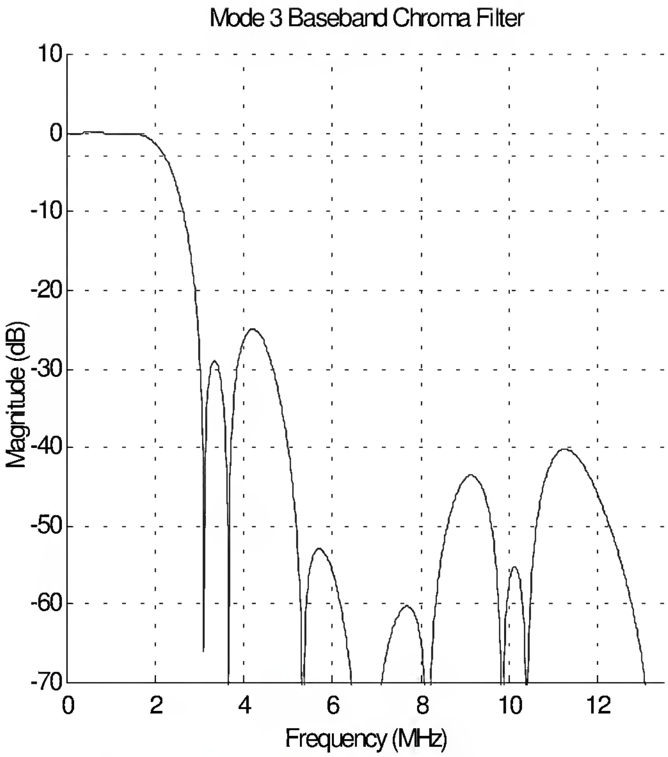
1.3MHz Low Pass Chroma Filter



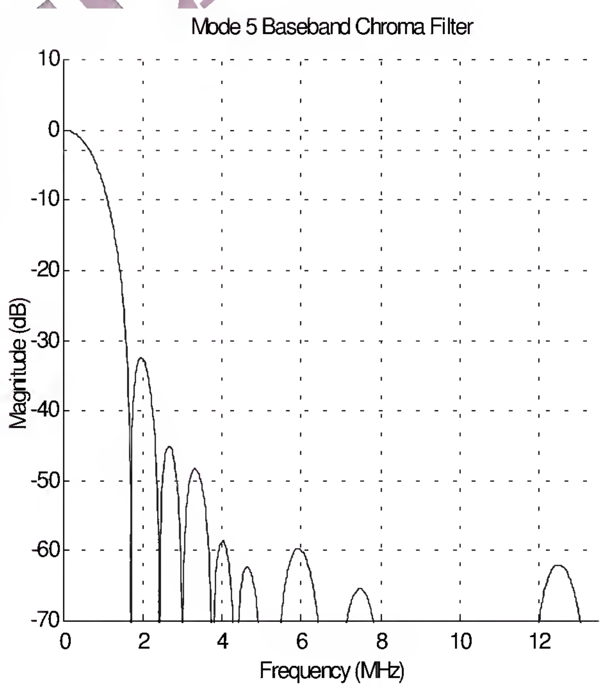
0.65MHz Low Pass Chroma Filter



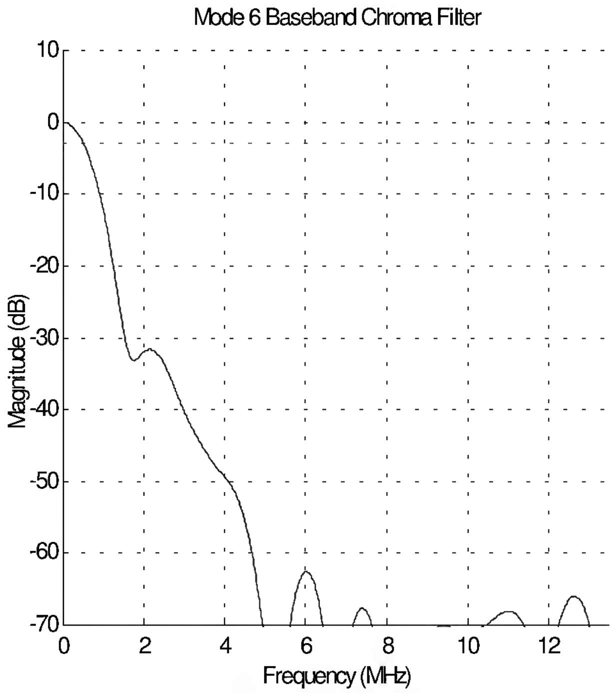
1.0MHZ Low Pass Chroma Filter



2.0MHz Low Pass Chroma Filter



CIF Chroma Filter



QCIF Chroma Filter

COLOR BAR GENERATION

The ADV7170/ADV7171 can be configured to generate 75% amplitude, 75% saturation (75/7.5/75/7.5) for NTSC or 75% amplitude, 100% saturation (100/0/75/0) for PAL color bars. These are enabled by setting MR17 of Mode Register 1 to logic "1".

SQUARE PIXEL MODE

The ADV7170/ADV7171 can be used to operate in square pixel mode. For NTSC operation an input clock of 24.5454MHz is required. Alternatively, for PAL operation, an input clock of 29.5MHz is required. The internal Timing logic adjusts accordingly for square pixel mode operation.

COLOR SIGNAL CONTROL

The color information can be switched on and off the video output using Bit MR24 of Mode Register 2.

BURST SIGNAL CONTROL

The burst information can be switched on and off the video output using Bit MR25 of Mode Register 2.

NTSC PEDESTAL CONTROL

The pedestal on both odd and even fields can be controlled on a line by line basis using the NTSC Pedestal Control Registers. This allows the pedestals to be controlled during the vertical blanking interval (lines 10 to 25 and lines 273 to 288).

PIXEL TIMING DESCRIPTION.

The ADV7170/ADV7171 can operate in eith 8-Bit or 16-Bit YCrCb Mode.

8-Bit YCrCb Mode

This default mode accepts multiplexed YCrCb inputs through the P7-P0 pixel inputs. The inputs follow the sequence Cb0, Y0 Cr0, Y1 Cb1, Y2, etc. The Y, Cb and Cr data are input on a rising clock edge.

16-Bit YCrCb Mode

This mode accepts Y inputs through the P7-P0 pixel inputs and multiplexed CrCb inputs through the P15-P8 pixel inputs. The data is loaded on every second rising clock edge of CLOCK. The inputs follow the sequence Cb0, Y0 Cr0, Y1 Cb1, Y2, etc.

SUBCARRIER RESET

Together with the SCRESET/RTC PIN and bits MR22 and MR21 of Mode Register 2, the ADV7170/ADV7171 can be used in subcarrier reset mode. The subcarrier will reset to field 0 at the start of the following field when a low to high transistion occurs on this input pin.

REAL TIME CONTROL

Together with the SCRESET/RTC PIN and bits MR22 and MR21 of Mode Register 2, the ADV7170/ADV7171 can be used to lock to an external video source. The real time control mode allows the ADV7170/ADV7171 to automatically alter the subcarrier frequency to compensate for line length variation. When the part is connected to a device that outputs out a digital datastream in the RTC format (such as a ADV7185 video decoder,see Figure 12), the part will automatically change to the compensated subcarrier frequency on a line by line basis. This digital datastream is 67 bits wide and the subcarrier is contained in bits 0 to 21. Each bit is 2 clock cycles long. 00Hex should be written into all four Subcarrier Frequency registers when using this mode.

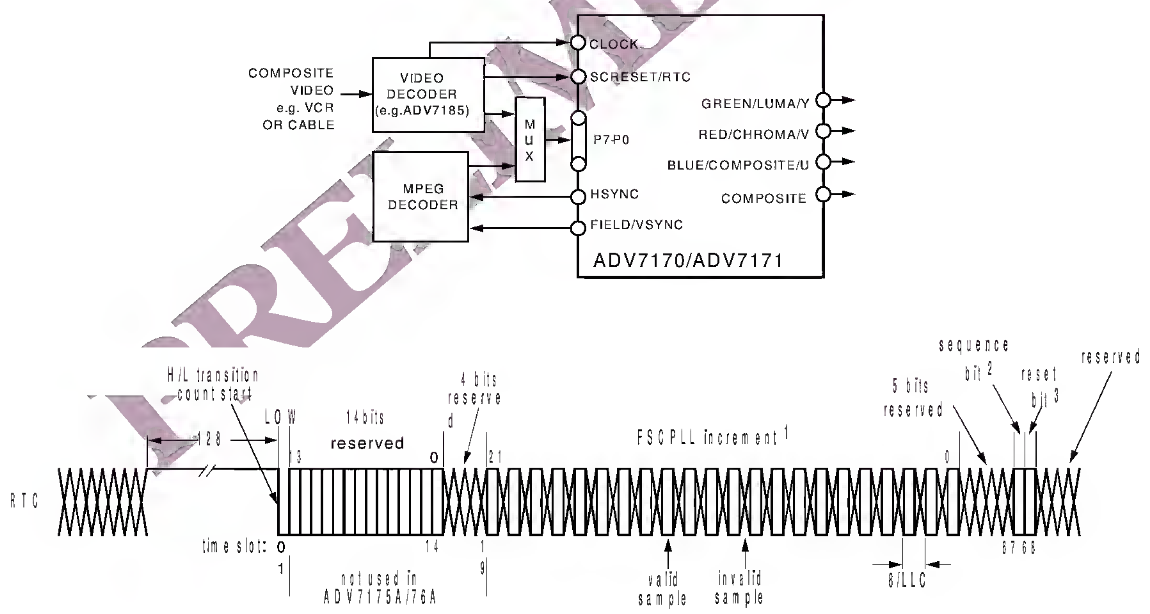
VIDEO TIMING DESCRIPTION.

The ADV7170/ADV7171 is intended to interface to off the shelf MPEG1 and MPEG2 Decoders. As a consequence the ADV7170/ADV7171 accepts 4:2:2 YCrCb Pixel Data via a CCIR-656 Pixel Port and has several Video Timing Modes of operation that allow it to be configured as either System Master Video Timing Generator or a Slave to the System Video Timing Generator. The ADV7170/ ADV7171 generates all of the required horizontal and vertical timing periods and levels for the Analog Video Outputs.

The ADV7170/ADV7171 calculates the width and placement of analog sync pulses, blanking levels and color burst envelopes. Color bursts are disabled on appropriate lines and serration and equalisation pulses are inserted where required.

In addition the ADV7170/ADV7171 supports a PAL or NTSC square pixel operation in slave mode. The part requires an input pixel clock of 24.5454MHz for NTSC and an input pixel clock of 29.5MHz for PAL. The internal horizontal line counters place the various video waveform sections in the correct location for the new clock frequencies.

The ADV7170/ADV7171 has 4 distinct Master and 4 distinct Slave timing configurations.Timing Control is establised with the bi-directional $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and FIELD/$\overline{\text{VSYNC}}$ pins. Timing Mode Register 1 can also be used to vary the timing pulse widths and the where they occur in relation to each other.



Notes:

1 Fsc PLL increment is 22 bits long, valued loaded into ADV7175A/76A Fsc DDS register is Fsc PLL incremnts bits 21:0 plus bits 0:9 of Sub Carrier Frequency Registers. All zeros should be written to the Sub Carrier Frequency Registers of the ADV7175A/76A.

2 Sequence bit
PAL: 0 = line normal, 1 = line inverted
NTSC : 0 = no change.

3 Reset bit
Reset ADV7175A/76A's DDS.

Figure 12. RTC Timing and Connections

Vertical Blanking Data Insertion

It is possible to allow encoding of imcoming YCbCr data on those lines of VBI that do not bear line sync or pre/post-equalisation pulses (see Figures 14 to 25). This mode of operation is called "Partial blanking" and this is selected by setting MR31 to 1. It allows the insertion of any VBI data(Opened VBI) into the encoded output waveform, this data is present in digitized incoming YCbCr data stream (e.g. WSS data, CGMS, VPS etc.). Alternatively the entire VBI may be blanked (no VBI data inserted) on these lines by setting MR31 to 0.

The complete VBI comprises of the following lines:
525/60 systems, lines 525 to 21 for field one and lines 262 to line 284 for field two.
625/50 systems, lines 624 to line 22 and lines 311 to 335.
The "Opened VBI" consists of:
525/60 systems, lines 10 to 21 for field one and second half of line 273 to line 284 for field two.
625/50 systems, line 7 to line 22 and lines 319 to 335.

Mode 0 (CCIR-656) :- Slave Option.
(Timing Register 0 TR0 = X X X X X 0 0 0)

The ADV7170/ADV7171 is controlled by the SAV (Start Active Video) and EAV (End Active Video) Time Codes in the Pixel Data. All timing information is transmitted using a 4-byte Synchronisation Pattern. A Synchronisation pattern is sent immediately before and after each line during Active Picture and Retrace. Mode 0 is illustrated in Figure 13. The $\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$ and $\overline{\text{BLANK}}$ (if not used) pins should be tied high during this mode.

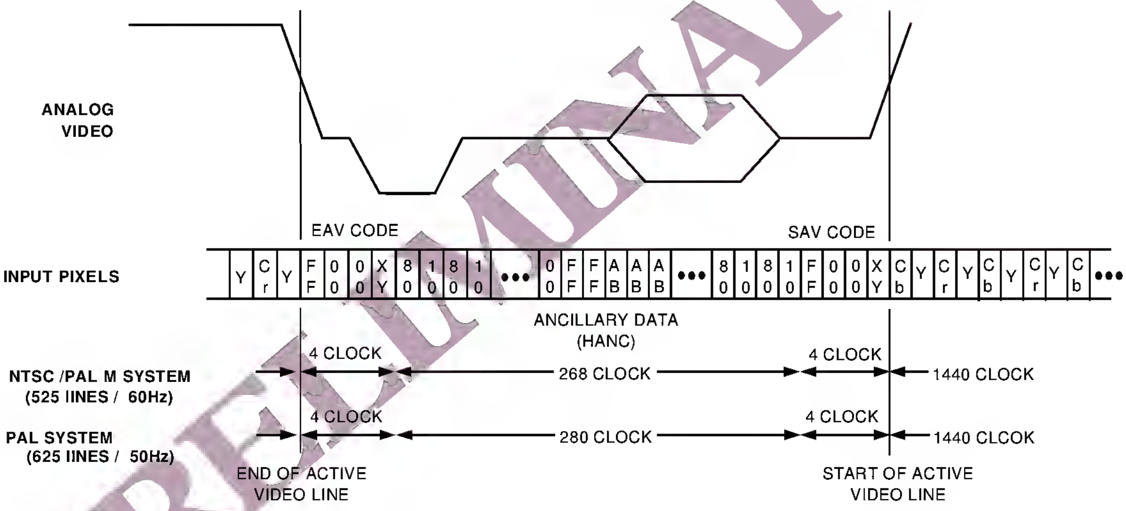


Figure 13. Timing Mode 0 (Slave Mode)

Mode 0 (CCIR-656) :- Master Option.
(Timing Register 0 TR0 = X X X X X 0 0 1)

The ADV7170/ADV7171 generates H, V and F signals required for the SAV (Start Active Video) and EAV (End Active Video) Time Codes in the CCIR656 standard. The H bit is output on the $\overline{\text{HSYNC}}$ pin, the V bit is output on the $\overline{\text{BLANK}}$ pin and the F bit is output on the FIELD/$\overline{\text{VSYNC}}$ pin. Mode 0 is illustrated in Figure 14 (NTSC) and Figure 15 (PAL). The H V and F transitions relative to the video waveform are illustrated in Figure 16.

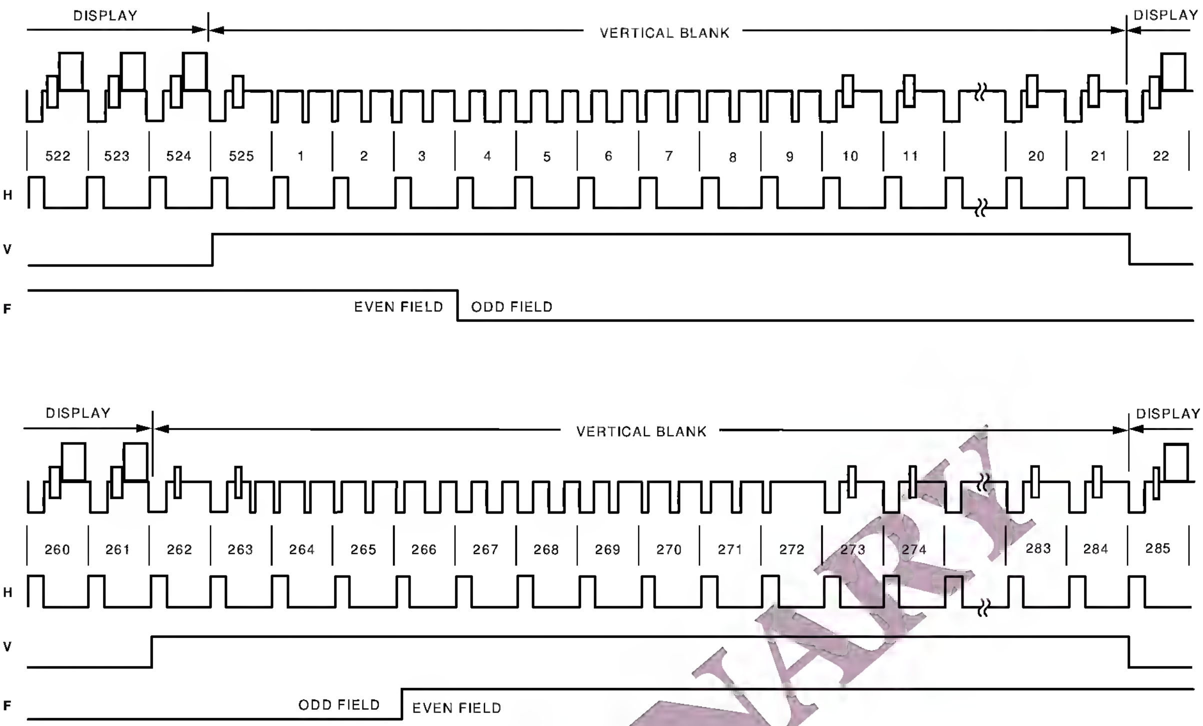


Figure 14. Timing Mode 0 (NTSC Master Mode)

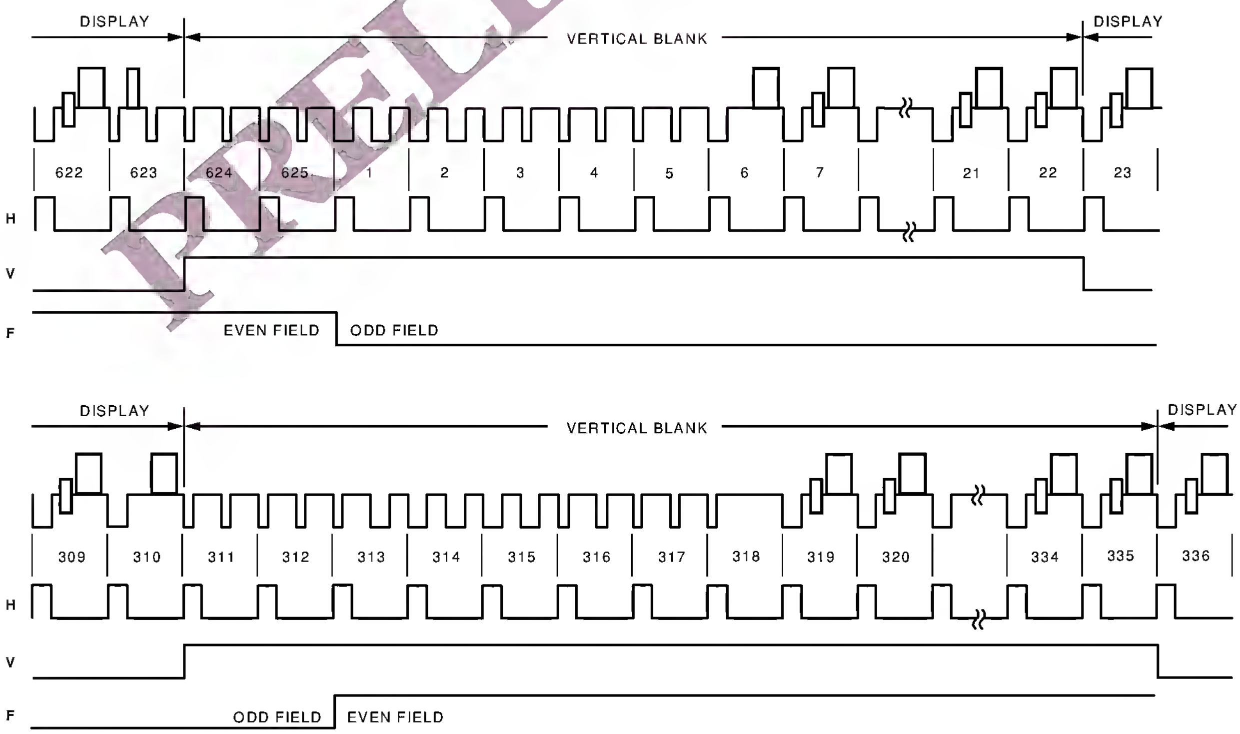


Figure 15. Timing Mode 0 (PAL Master Mode)

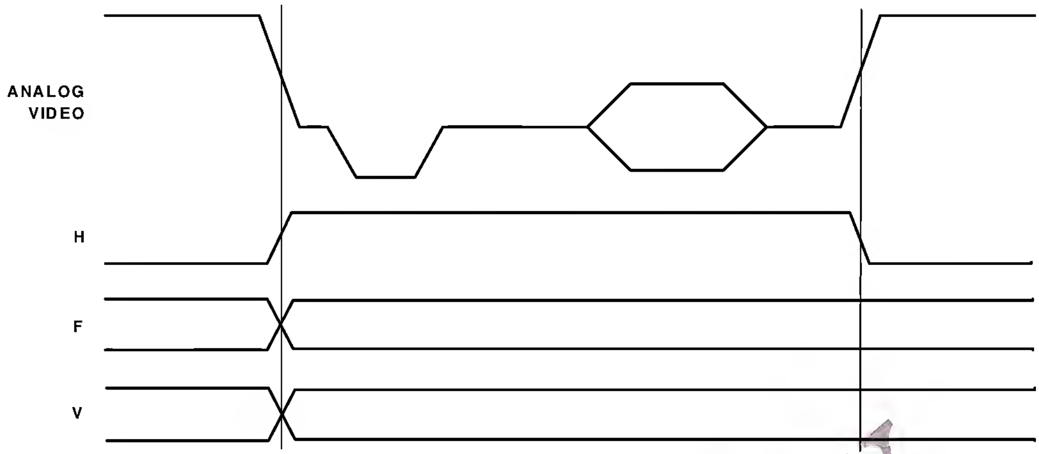


Figure 16. Timing Mode 0 Data Transitions (Master Mode)

Mode 1 :- Slave Option. $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD.
(Timing Register 0 TR0 = X X X X X 0 1 0)

In this mode the ADV7170/ADV7171 accepts Horizontal SYNC and Odd/ Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame i.e. Vertical Retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7170/ADV7171 automatically blanks all normally blank . Mode 1 is illustrated in Figure 17 (NTSC) and Figure 18 (PAL).

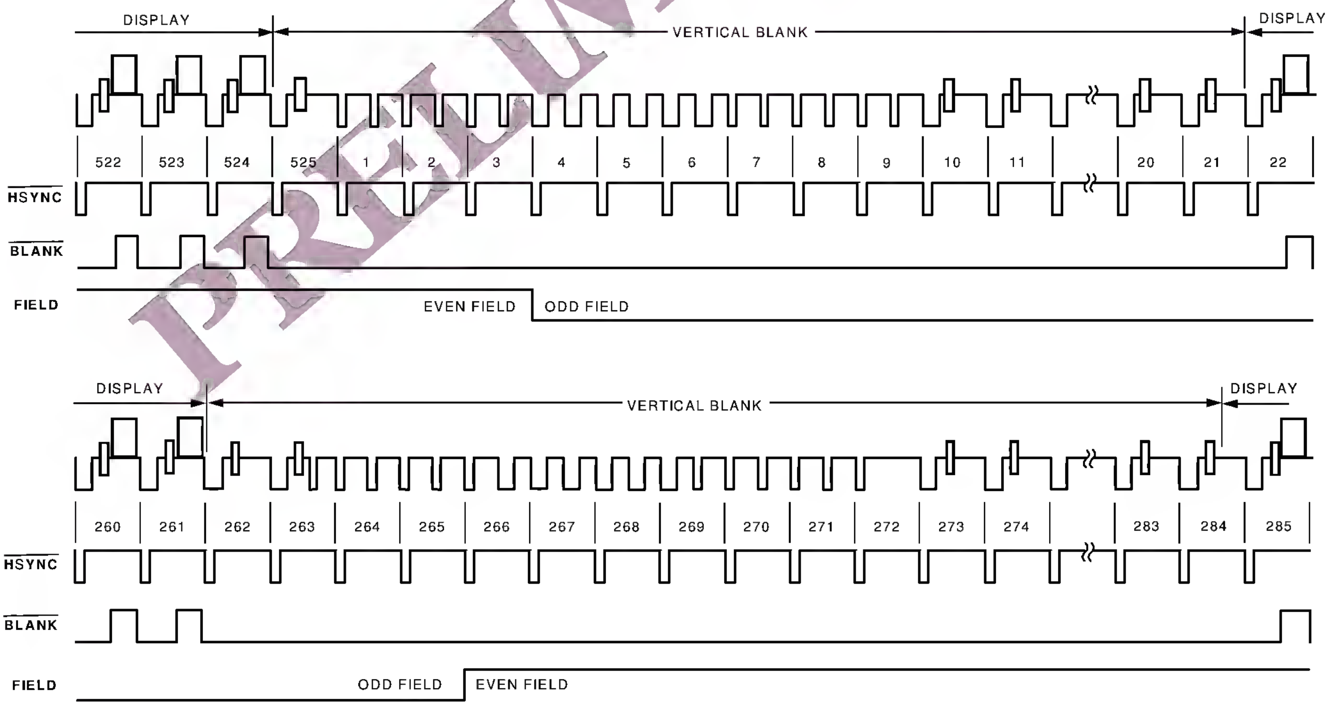


Figure 17. Timing Mode 1 (NTSC)

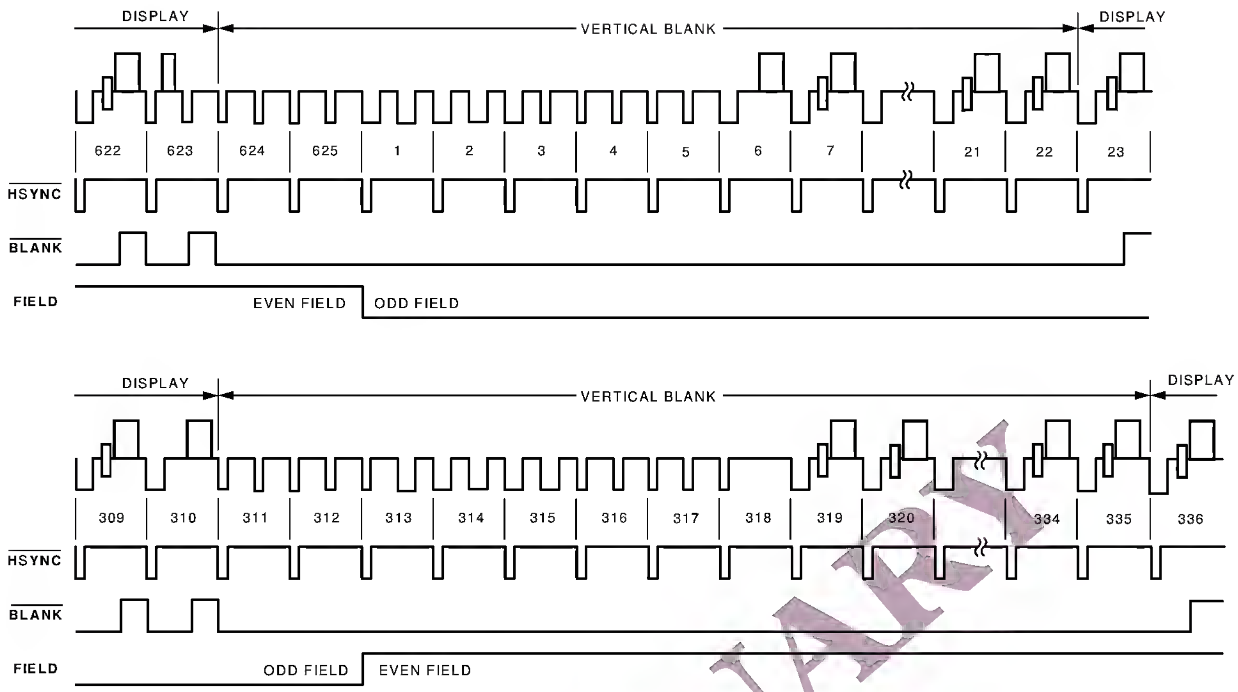


Figure 18. Timing Mode 1 (PAL)

Mode 1 :- Master Option. $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD.
(Timing Register 0 TR0 = X X X X X 0 1 1)

In this mode the ADV7170/ADV7171 can generate Horizontal SYNC and Odd / Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame i.e. Vertical Retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7170/ADV7171 automatically blanks all normally blank lines . Pixel data is latched on the rising clock edge following the timing signal transitions. Mode 1 is illustrated in Figure 17 (NTSC) and Figure 18 (PAL). Figure 19 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$ and FIELD for an odd or even field transition relative to the pixel data.

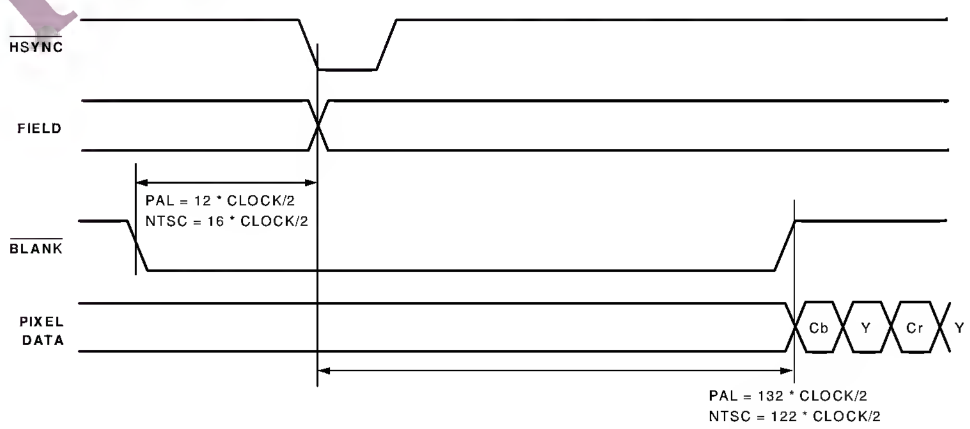


Figure 19 Timing Mode 1 Odd/Even Field Transitions Master/Slave

Mode 2 :- Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$.
(Timing Register 0 TR0 = X X X X X 1 0 0)

In this mode the ADV7170/ADV7171 accepts Horizontal and Vertical SYNC signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an Odd Field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an Even Field. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7170/ADV7171 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 20 (NTSC) and Figure 21 (PAL).

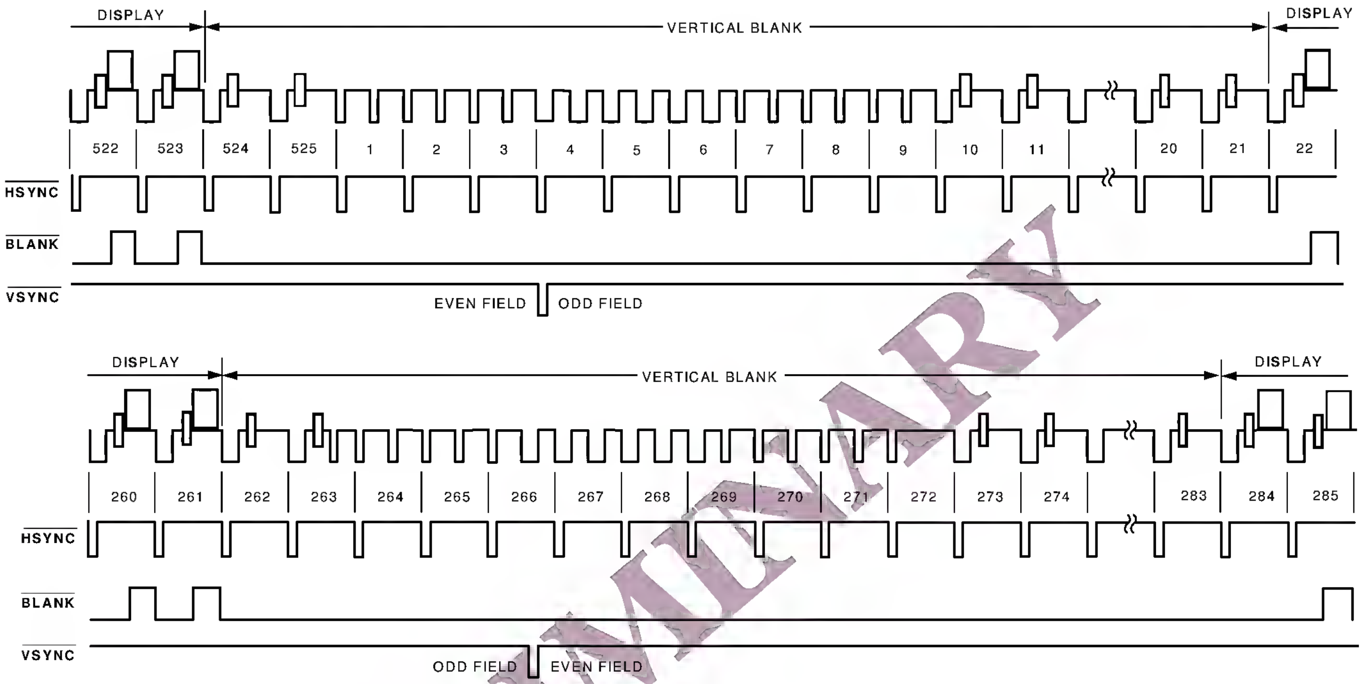


Figure 20. Timing Mode 2 (NTSC)

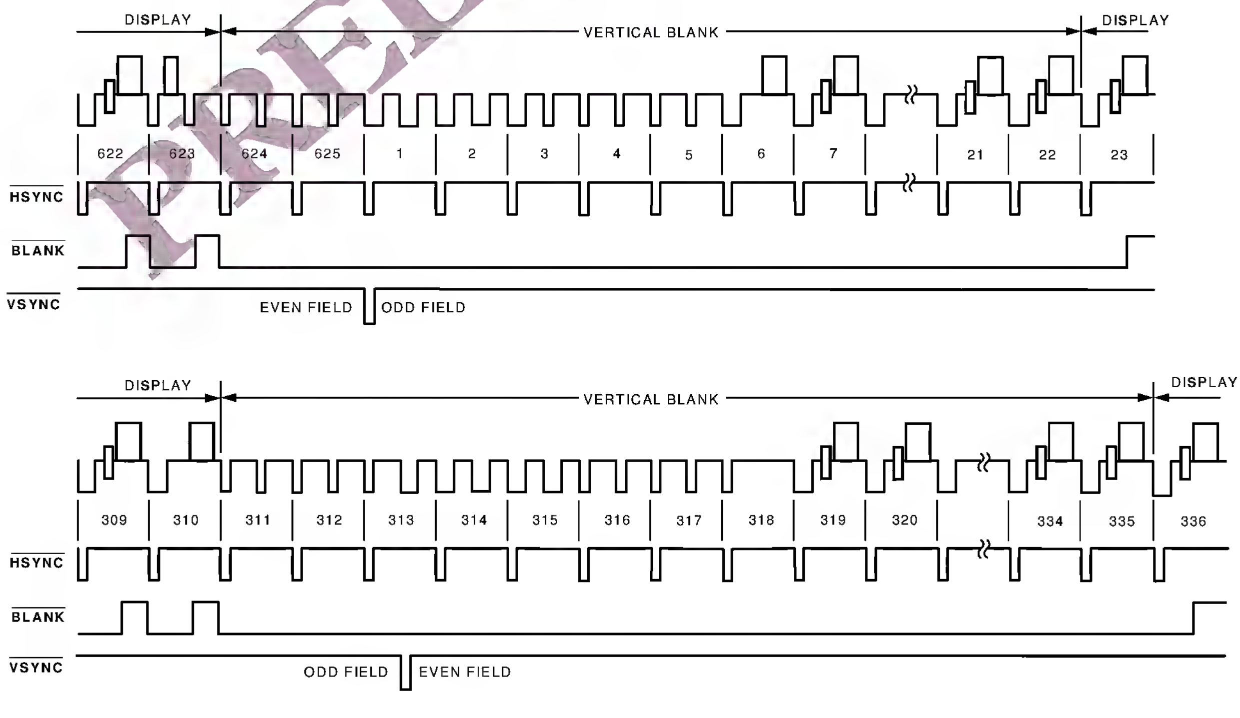


Figure 21. Timing Mode 2 (PAL)

Mode 2 :- Master Option $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$.
(Timing Register 0 TR0 = X X X X X 1 0 1)

In this mode the ADV7170/ADV7171 can generate Horizontal and Vertical SYNC signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an Odd Field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an Even Field. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7170/ADV7171 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is

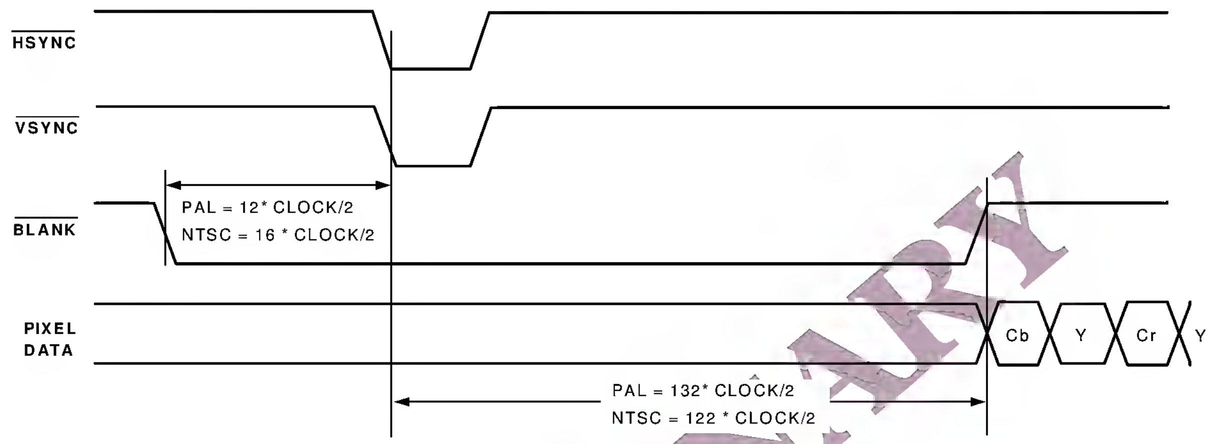


Figure 22. Timing Mode 2 Even to Odd Field Transistion Master/Slave

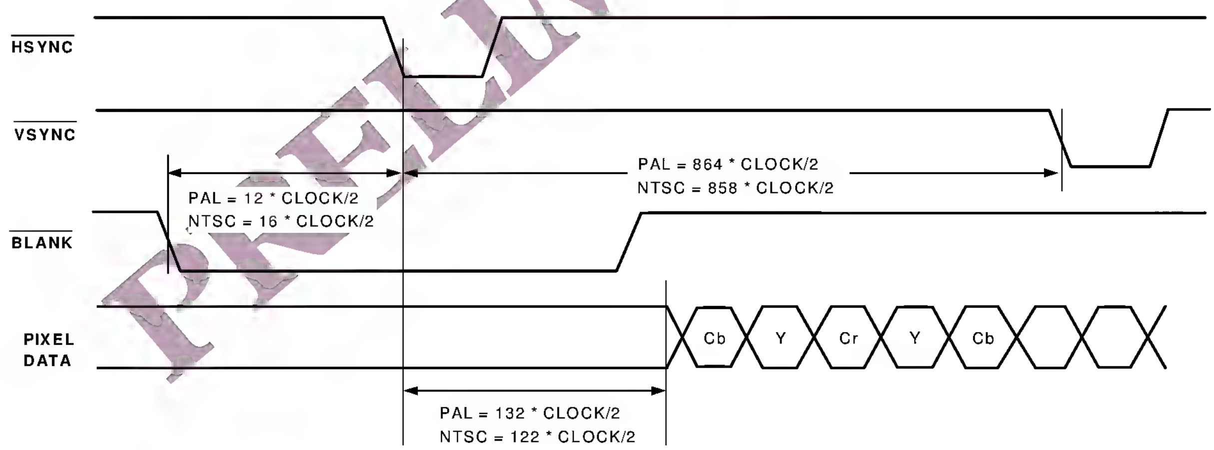


Figure 23. Timing Mode 2 Odd to Even Field Transistion Master/Slave

Mode 3 :- Master/Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD.
(Timing Register 0 TR0 = X X X X X 1 1 0 or X X X X X 1 1 1)

In this mode the ADV7170/ADV7171 accepts or generates Horizontal SYNC and Odd / Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is high indicates a new frame i.e. Vertical Retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7170/ADV7171 automatically blanks all normally blank lines as per CCIR-624. Mode 3 is illustrated in Figure 24 (NTSC) and Figure 25 (PAL).

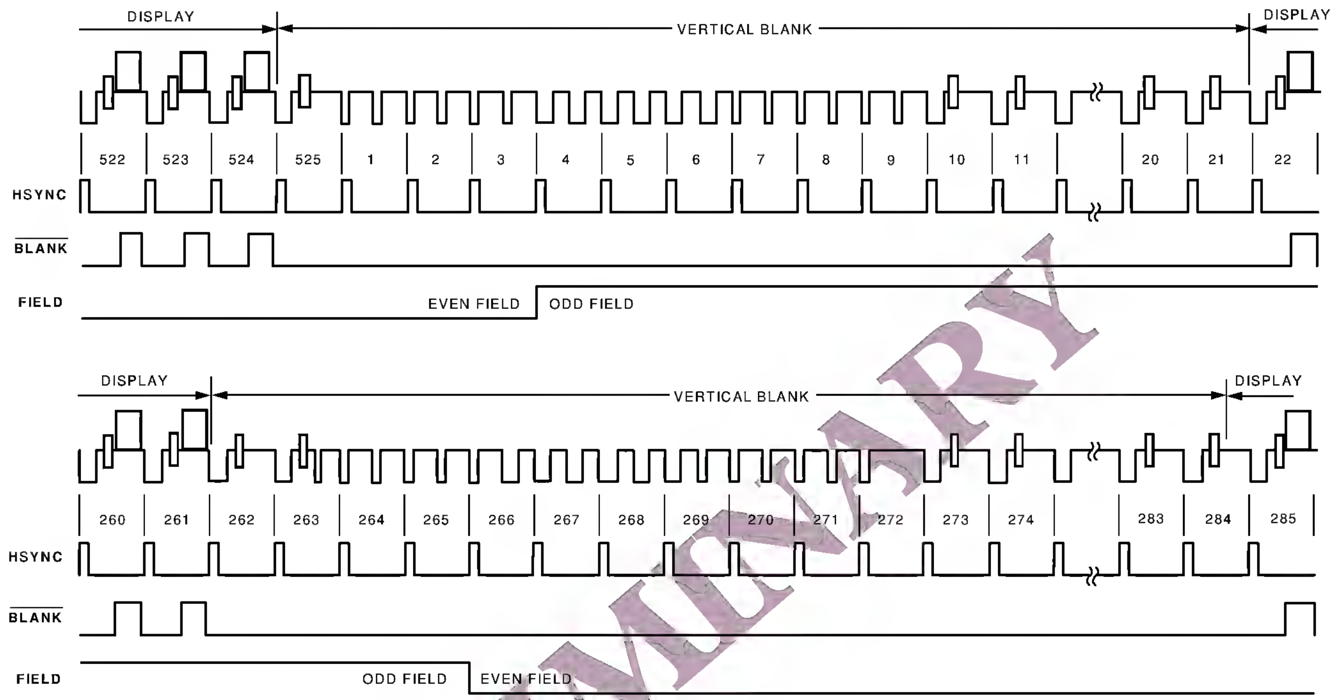


Figure 24. Timing Mode 3 (NTSC)

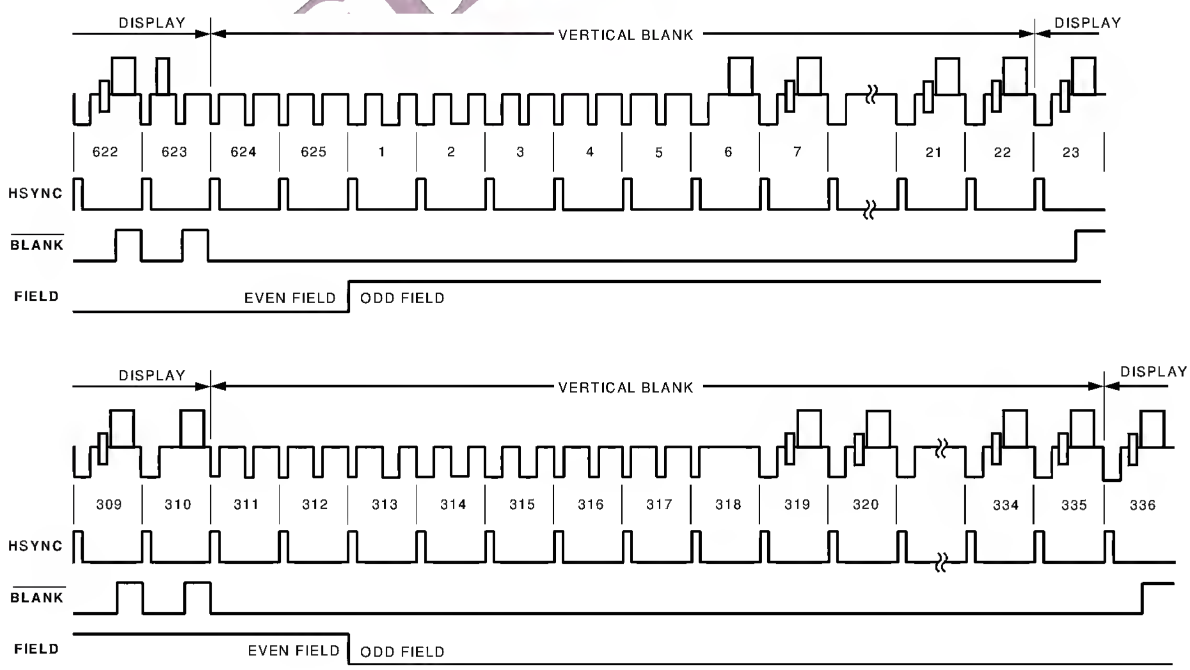


Figure 25. Timing Mode 3 (PAL)

OUTPUT VIDEO TIMING

The Video Timing Generator generates the appropriate SYNC, BLANK and BURST sequence that controls the output analog waveforms. These sequences are sumarised below. In slave modes the following sequences are synchronised with the input timing control signals. In master modes the timing generator free runs and generates the following sequences in addition to the output timing control signals.

NTSC - Interlaced :Scan Lines 1-9 and 264-272 are always blanked and vertical sync pulses are included. Scan Lines 525, 10-21 and 262, 263, 273-284 are also blanked and can be used for closed captioning data. Burst is disabled on lines 1-6, 261-269 and 523-525.

NTSC- Non-Interlaced :Scan Lines 1-9 are always blanked and vertical sync pulses are included. Scan Lines 10-21 are also blanked and can be used for closed captioning data. Burst is disabled on lines 1-6, 261-262.

PAL- Interlaced :Scan Lines 1-6, 311-318 and 624-625 are always blanked and vertical sync pulses are included in Fields 1, 2, 5 & 6. Scan Lines 1-5, 311-319 and 624-625 are always blanked and vertical sync pulses are included in Fields 3, 4, 7 & 8. The remaining Scan Lines in the Vertical Blanking interval are also blanked and can be used for teletext data. Burst is disabled on lines 1-6, 311-318 and 623-625 in Fields 1, 2, 5 & 6. Burst is disabled on lines 1-5, 311-319 and 623-625 in Fields 3, 4, 7 & 8.

PAL- Non-Interlaced :Scan Lines 1-6 and 311-312 are always blanked and vertical sync pulses are included. The remaining Scan Lines in the Vertical Balnking Interval are also blanked and can be used for Teletext data. Burst is disabled on lines 1-5, 310-312.

POWER-ON RESET

After power-up, it is necessary to execute a reset operation. A reset occurs on the falling edge of a high to low transistion on the $\overline{\text{RESET}}$ pin. This initializes the pixel port such that the pixel inputs P7-P0 are selected. After reset, the ADV7170/ADV7171 is automatically set up to operate in NTSC Mode. Subcarrier frequency code 21F07C16 HEX is loaded into the Sub-Carrier Frequency registers. All other registers, with the exception of Mode Register 0, are set to 00H. All bits in Mode Register 0 are set to logic level "0" except Bit MR02. Bit MR02 of Mode Register 0 is set to logic "1". This enables the 7.5IRE pedestal.

SCH Phase mode

The SCH phase is configured in default mode to reset every four(NTSC) or eight(PAL) fields to avoid an accumulation of SCH phase error over time. In an ideal system, zero SCH phase error would be maintained forever, but in reality, this is impossible to achieve due to clock frequency variations. This is effect is reduced by the use of a 32-bit DDS, which generates this SCH.

Resetting the SCH phase every four or eight fields avoids the accumulation of SCH phase error, and results in very minor SCH phase jumps at the start of the four or eight field sequence.

Resetting the SCH phase should not be done if the video source does not have stable timimg or the ADV7170/76A is configured in RTC mode (MR22= 1 and MR22=1). Under these conditions (unstable video) the Subcarrier Phase Reset should be enabled(MR22=0 and MR21=1) but no reset applied. In this configuration the SCH Phase will never be reset, this means that the output video will now track the unstable input video. The Subcarrier Phase Reset when applied will reset the SCH phase to field 0 at the start of the next field(e.g. Subcarrier Phase Reset applied in Field 5(PAL) on the start of the next field SCH phase will be reset to field 0).

MPU PORT DESCRIPTION.

The ADV7170 and ADV7171 support a two wire serial (I^2C Compatible) microprocessor bus driving multiple peripherals. Two inputs Serial Data (SDATA) and Serial Clock (SCLOCK) carry information between any device connected to the bus. Each slave device is recognised by a unique address. The ADV7170 and ADV7171 each have four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 26 and Figure 27. The LSB sets either a read or write operation. Logic level "1" corresponds to a read operation while logic level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7170/ADV7171 to logic level "0" or logic level "1".

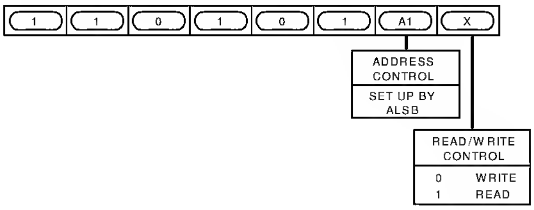


Fig 26. ADV7170 Slave Address

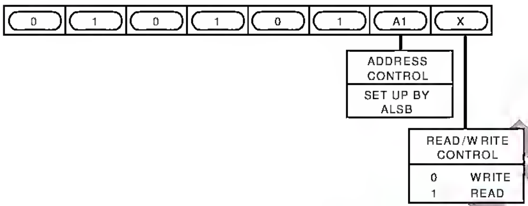


Fig 27. ADV7171 Slave Address

To control the various devices on the bus the following protocol must be followed. First the master initiates a data transfer by establishing a Start condition, defined by a high to low transistion on SDATA whilst SCLOCK remains high. This indicates that an address/data stream will follow. All peripherals respond to the Start condition and shift the next eight bits (7-Bit address + R/$\overline{W}$ bit). The bits tranferred from MSB down to LSB. The peripheral that recognises the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDATA and SCLOCK lines waiting for the Start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data. A logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7170/ADV7171 acts as a standard slave device on the bus. The data on the SDATA pin is 8 bits long supporting the 7-Bit addresses plus the R/$\overline{W}$ bit. The ADV7170 has 33 subaddresses and the ADV7171 has 19 subaddresses to enable access to the internal registers. It therefore interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto increment allowing data to be written to or read from from the starting subaddress. A data transfer is always terminated by a Stop condition. The user can also access any unique subaddress register on a one by one basis without having to update all the registers. There is one exception. The Sub-Carrier Frequency Registers should be updated in sequence, starting with Sub-Carrier Frequency Register 0. The auto increment function should be then used to increment and access Sub-Carrier Frequency Registers 1, 2 and 3. The Sub-Carrier Frequency Registers should not be accessed independently.

Stop and Start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, then these cause an immediate jump to the idle condition. During a given SCLOCK high period the user should only issue one Start condition, one Stop condition or a single Stop condition followed by a single Start condition. If an invalid subaddress is issued by the user, the ADV7170/ADV7171 will not issue an acknowledge and will return to the idle condition. If in auto-increment mode, the user exceeds the highest subaddress then the following action will be taken:

1. In Read Mode the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDATA line is not pulled low on the ninth pulse.

2. In Write Mode, the data for the invalid byte will be not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7170/ADV7171 and the part will return to the idle condition.

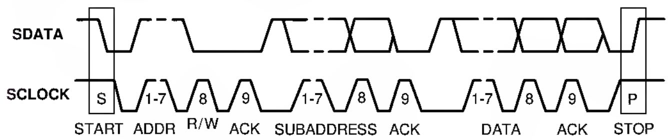


Figure 28. Bus Data Transfer

Figure 28 illustrates an example of data transfer for a read sequence and the Start and Stop conditions.

Figure 29 shows bus write and read sequences.

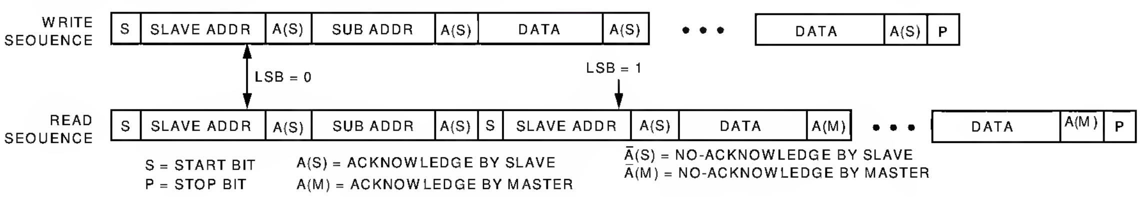


Figure 29. Write and Read Sequences

REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7170/ADV7171 except the Subaddress Register which is a write only register. The Subaddress Register determines which register the next read or write operation accesses. All communications with the part through thebus start with an access to the Subaddress Register. Then a read/write operation is performed from/to the target address which then increments to the next address until a Stop command on the bus is performed.

REGISTER PROGRAMMING

The following section describes each register, including Subaddress Register, Mode Registers, Sub-Carrier Frequency Registers, Sub-Carrier Phase Register, Timing Registers, Closed Captioning Extended Data Registers, Closed Captioning Data Registers and NTSC Pedestal Control Registers in terms of its configuration.

Subaddress Register (SR7-SR0)

The Communications Register is an eight bit write-only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress set up. The Subaddress Register determines to/from which register the operation takes place.

Figure 30 shows the various operations under the control of the Subaddress Register. Zero should always be written to SR7-SR6.

Register Select (SR5-SR0):

These bits are set up to point to the required starting address.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

SR7-SR 5 (000)
ZERO SHOULD BE WRITTEN TO THESE BITS

ADV7171 SUBADDRESS REGISTER

SR5	SR4	SR3	SR2	SR1	SR0	
0	0	0	0	0	0	MODE REGISTER 0
0	0	0	0	0	1	MODE REGISTER 1
0	0	0	0	1	0	MODE REGISTER 2
0	0	0	0	1	1	MODE REGISTER 3
0	0	0	1	0	0	MODE REGISTER 4
0	0	0	1	0	1	RESERVED
0	0	0	1	1	0	RESERVED
0	0	0	1	1	1	TIMING MODE REGISTER 0
0	0	1	0	0	0	TIMING MODE REGISTER 1
0	0	1	0	0	1	SUB CARRIER FREQUENCY REGISTER 0
0	0	1	0	1	0	SUB CARRIER FREQUENCY REGISTER 1
0	0	1	0	1	1	SUB CARRIER FREQUENCY REGISTER 2
0	0	1	1	0	0	SUB CARRIER FREQUENCY REGISTER 3
0	0	1	1	0	1	SUB CARRIER PHASE REGISTER
0	0	1	1	1	0	CLOSED CAPTIONING EXTENDED DATA-BYTE 0
0	0	1	1	1	1	CLOSED CAPTIONING EXTENDED DATA-BYTE 1
0	1	0	0	0	0	CLOSED CAPTIONING DATA-BYTE 0
0	1	0	0	0	1	CLOSED CAPTIONING DATA-BYTE 1
0	1	0	0	1	0	NTSC PEDESTAL CONTROL REG 0
0	1	0	0	1	1	NTSC PEDESTAL CONTROL REG 1
0	1	0	1	0	0	NTSC PEDESTAL CONTROL REG 2
0	1	0	1	0	1	NTSC PEDESTAL CONTROL REG 3
0	1	0	1	1	0	CGMS_WSS_0
0	1	0	1	1	1	CGMS_WSS_1
0	1	1	0	0	0	CGMS_WSS_2
0	1	1	0	0	1	TELETEXT REQUEST POSITION

ADV7170 SUBADDRESS REGISTER

SR5	SR4	SR3	SR2	SR1	SR0	
0	0	0	0	0	0	MODE REGISTER 0
0	0	0	0	0	1	MODE REGISTER 1
0	0	0	0	1	0	MODE REGISTER 2
0	0	0	0	1	1	MODE REGISTER 3
0	0	0	1	0	0	MODE REGISTER 4
0	0	0	1	0	1	RESERVED
0	0	0	1	1	0	RESERVED
0	0	0	1	1	1	TIMING MODE REGISTER 0
0	0	1	0	0	0	TIMING MODE REGISTER 1
0	0	1	0	0	1	SUB CARRIER FREQUENCY REGISTER 0
0	0	1	0	1	0	SUB CARRIER FREQUENCY REGISTER 1
0	0	1	0	1	1	SUB CARRIER FREQUENCY REGISTER 2
0	0	1	1	0	0	SUB CARRIER FREQUENCY REGISTER 3
0	0	1	1	0	1	SUB CARRIER PHASE REGISTER
0	0	1	1	1	0	CLOSED CAPTIONING EXTENDED DATA-BYTE 0
0	0	1	1	1	1	CLOSED CAPTIONING EXTENDED DATA-BYTE 1
0	1	0	0	0	0	CLOSED CAPTIONING DATA-BYTE 0
0	1	0	0	0	1	CLOSED CAPTIONING DATA-BYTE 1
0	1	0	0	1	0	NTSC PEDESTAL CONTROL REG 0
0	1	0	0	1	1	NTSC PEDESTAL CONTROL REG 1
0	1	0	1	0	0	NTSC PEDESTAL CONTROL REG 2
0	1	0	1	0	1	NTSC PEDESTAL CONTROL REG 3
0	1	0	1	1	0	CGMS_WSS_0
0	1	0	1	1	1	CGMS_WSS_1
0	1	1	0	0	0	CGMS_WSS_2
0	1	1	0	0	1	TELETEXT REQUEST POSITION
0	1	1	0	1	0	RESERVED
0	1	1	0	1	1	RESERVED
0	1	1	1	0	0	RESERVED
0	1	1	1	0	1	RESERVED
0	1	1	1	1	0	MACRO VISION REGISTERS
0	1	1	1	1	1	MACRO VISION REGISTERS
1	0	0	0	0	0	MACRO VISION REGISTERS
1	0	0	0	0	1	MACRO VISION REGISTERS
1	0	0	0	1	0	MACRO VISION REGISTERS
1	0	0	0	1	1	MACRO VISION REGISTERS
1	0	0	1	0	0	MACRO VISION REGISTERS
1	0	0	1	0	1	MACRO VISION REGISTERS
1	0	0	1	1	0	MACRO VISION REGISTERS
1	0	0	1	1	1	MACRO VISION REGISTERS
1	0	1	0	0	0	MACRO VISION REGISTERS
1	0	1	0	0	1	MACRO VISION REGISTERS
1	0	1	0	1	0	MACRO VISION REGISTERS
1	0	1	0	1	1	MACRO VISION REGISTERS
1	0	1	1	0	0	MACRO VISION REGISTERS
1	0	1	1	0	1	MACRO VISION REGISTERS
1	0	1	1	1	0	MACRO VISION REGISTERS
1	0	1	1	1	1	MACRO VISION REGISTERS

Figure 30. Subaddress Register

MODE REGISTER 0 MR0 (MR07-MR00)
(Address (SR4-SR0) = 00H)

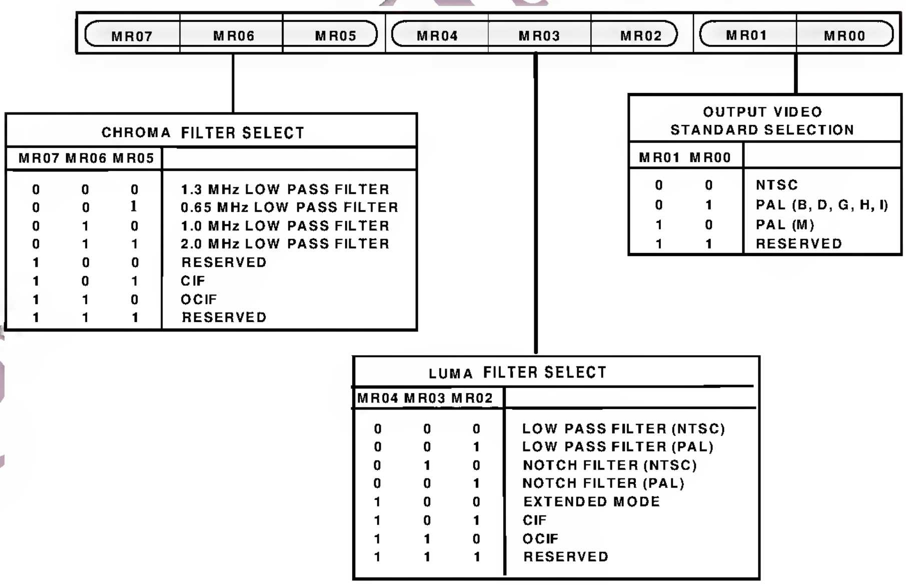
Figure 31 shows the various operations under the control of Mode Register 0. This register can be read from as well written to.

-MR0 BIT DESCRIPTION-

Encode Mode Control (MR01-MR00):
These bits are used to setup the encoder mode. The ADV7170/ADV7171 can be set up to output NTSC, PAL (B,D,G,H,I), PAL(M) standard video.

Luminance Filter Control (MR02-MR04):
These bits specify which luma filter is to be selected. The filter selection is made independent of whether PAL or NTSC is selected.

Chrominance Filter Control (MR05-MR07):
These bits select the chrominance filter. A low pass filter can be selected with a choice of cut-off frequencies, 0.65MHz, 1.0MHz, 1.3MHz or 2MHz along with a choice of CIF or QCIF filters.



CHROMA FILTER SELECT

MR07	MR06	MR05	
0	0	0	1.3 MHz LOW PASS FILTER
0	0	1	0.65 MHz LOW PASS FILTER
0	1	0	1.0 MHz LOW PASS FILTER
0	1	1	2.0 MHz LOW PASS FILTER
1	0	0	RESERVED
1	0	1	CIF
1	1	0	OCIF
1	1	1	RESERVED

OUTPUT VIDEO STANDARD SELECTION

MR01	MR00	
0	0	NTSC
0	1	PAL (B, D, G, H, I)
1	0	PAL (M)
1	1	RESERVED

LUMA FILTER SELECT

MR04	MR03	MR02	
0	0	0	LOW PASS FILTER (NTSC)
0	0	1	LOW PASS FILTER (PAL)
0	1	0	NOTCH FILTER (NTSC)
0	0	1	NOTCH FILTER (PAL)
1	0	0	EXTENDED MODE
1	0	1	CIF
1	1	0	OCIF
1	1	1	RESERVED

Figure 31. Mode Register 0 (MR0)

MODE REGISTER 1 MR1 (MR17-MR10)
(Address (SR4-SR0) = 01H)

Figure 32 shows the various operations under the control of Mode Register 1. This register can be read from as well written to.

-MR1 BIT DESCRIPTION-

Interlaced Mode Control (MR10):
This bit is used to setup the output to interlaced or non-interlaced mode. This mode is only relevant when the part is in composite video mode.

Closed Captioning Field Control (MR12-MR11)
These bits control the field that close captioning data is displayed on close captioning information can be displayed on an odd field, even field or both fields.

DAC Control (MR16-MR13):
These bits can be used to power down the DACs. This can be used to reduce the power consumption of the ADV7170/ADV7171 if any of the DACs are not required in the application.

Color Bar Control (MR17):
This bit can be used to generate and output an internal color bar test pattern. The color bar configuration is 75/7.5/75/7.5 for NTSC and 100/0/75/0 for PAL. It is imortant to note that when color bars are enabled the ADV7170/ADV7171 is configured in a Master Timimg mode as per the one selected by bits TR01 and TR02.

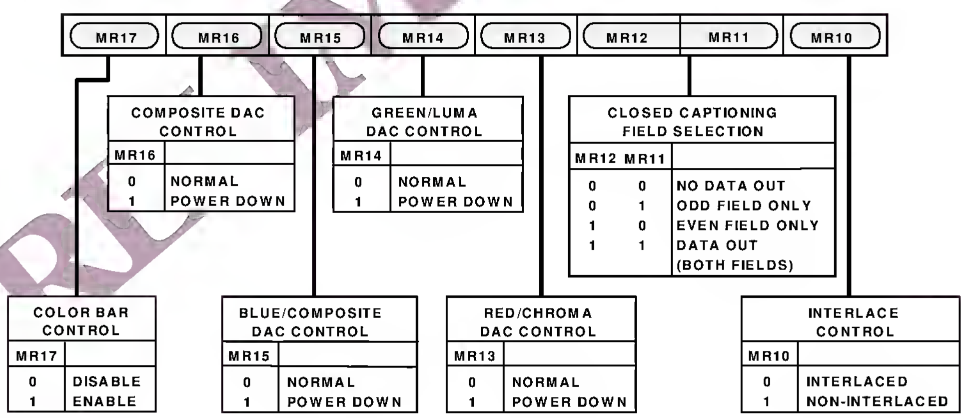


Figure 32. Mode Register 1 (MR1)

MODE REGISTER 2 MR2 (MR27-MR20)
(Address (SR4-SR0) = 02H)

Mode Register 2 is a 8-Bit wide register.

Figure 33 shows the various operations under the control of Mode Register 2. This register can be read from as well written to.

- MR2 BIT DESCRIPTION -

Square Pixel Mode Control (MR20):
This bit is used to setup square pixel mode. This is available in slave mode only. For NTSC, a 24.54MHz clock must be supplied. For PAL, a 29.5MHz clock must be supplied.

Genlock Control (MR22-MR21)
These bits control the genlock feature of the ADV7170/ADV7171. Setting MR21 to a logic "1" configures the SCRESET/RTC pin as an input. Setting MR22 to logic level "0" configures the SCRESET/RTC pin as a subcarrier reset input. Therefore the subcarrier will reset to field 0 following a high to low transition on the SCRESET/RTC pin. Setting MR22 to logic level "1" configures the SCRESET/RTC pin as a real time control input.

CCIR624/CCIR601 Control (MR23)
This bit switches between two active video line durations. A zero selects ITU-R BT.470(720 pixels PAL/NTSC) and a one selects ITU-R/SMPTE 'analog' standard for active video duration (710 pixels NTSC 702 pixels PAL).

Chrominance Control (MR24)
This bit enables the color information to be switched on and off the video output.

Burst Control (MR25)
This bit enables the burst information to be switched on and off the video output.

Low Power Control (MR26)
This bit enables the lower power mode of the ADV7170/ADV7171. This will reduce the DAC current by 20 %.

Reserved (MR27)
A logical 0 must be written to this bit

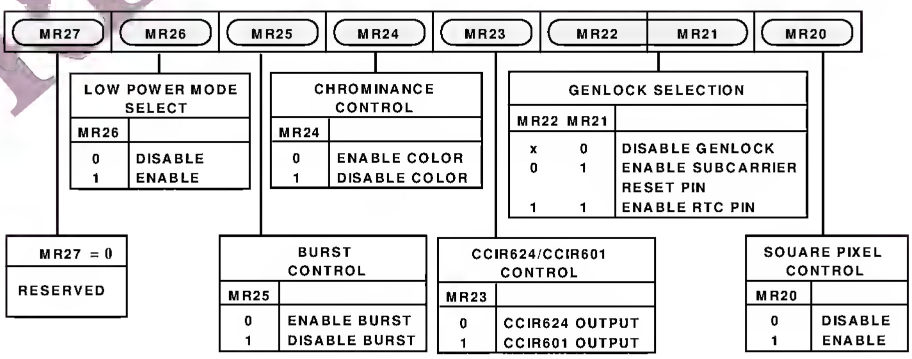


Figure 33. Mode Register 2

MODE REGISTER 3 MR3 (MR37-MR30)
(Address (SR4-SR0) = 03H)

Mode Register 3 is a 8-Bit wide register.
Figure 34 shows the various operations under the control of Mode Register 3.

-MR3 BIT DESCRIPTION-

Revision Code (MR30 - MR31):
This bit is read only and indicates the revision of the device.

VBI Passthrough Control (MR32):
This bit determines whether or not data in the Vertical Blanking Interval (VBI) is output to the analog outputs or blanked.

DAC Switching Control (MR33):
This bit is used to switch the DAC outputs from SCART to a EUROSCART configuration. A complete table of all DAC output configurations is shown below.

Chroma Output Select (MR34):
With this active high bit it is possible to output YUV data with a composite output on the fourth DAC or a chroma output on the fouirth DAC (0 = CVBS ; 1 = CHROMA)

Teletext Enable (MR35):
This bit must be set to "1" to enable teletext data insertion on the TTX pin.

Teletext Mode Control (MR36):
This bit enables switching of the teletext request signal from a continuous high signal("MR36 = 0") to a bitwise request signal ("MR36 = 1").

Input Default Color Control (MR37):
This bit determines the default output color from the DACs for zero input data (or disconnected). A logical "0" means that the color corresponding to 00000000 will be displayed. A logical "1" forces the output color to black for 00000000 input video data.

MR34	MR40	MR41	MR33	DAC A	DAC B	DAC C	DAC D	Simultaneous Output
0	0	0	0	CVBS	CVBS	C	Y	2 Composite and Y/C
0	0	0	1	Y	CVBS	C	CVBS	2 Composite and Y/C
0	0	1	0	CVBS	CVBS	C	Y	2 Composite and Y/C
0	0	1	1	Y	CVBS	C	CVBS	2 Composite and Y/C
0	1	0	0	CVBS	B	R	G	RGB & Composite
0	1	0	1	G	B	R	CVBS	RGB & Composite
0	1	1	0	CVBS	U	V	Y	YUV & Composite
0	1	1	1	Y	U	V	CVBS	YUV & Composite
1	0	0	0	C	CVBS	C	Y	1 Composite, Y & 2C
1	0	0	1	Y	CVBS	C	C	1 Composite, Y & 2C
1	0	1	0	C	CVBS	C	Y	1 Composite, Y & 2C
1	0	1	1	Y	CVBS	C	C	1 Composite, Y & 2C
1	1	0	0	C	B	R	G	RGB & C
1	1	0	1	G	B	R	C	RGB & C
1	1	1	0	C	U	V	Y	YUV & C
1	1	1	1	Y	U	V	C	YUV & C

CVBS: Composite Vide Baseband Signal
Y: Luminance Component Signal (For YUV or Y/C Mode)
C: Chrominance Signal (For Y/C Mode)
U: Chrominance Component Signal (For YUV Mode)
V: Chrominance Component Signal (For YUV Mode)
R: RED Component Video (For RGB Mode)
G: GREEN Component Video (For RGB Mode)
B: BLUE Component Video (For RGB Mode)

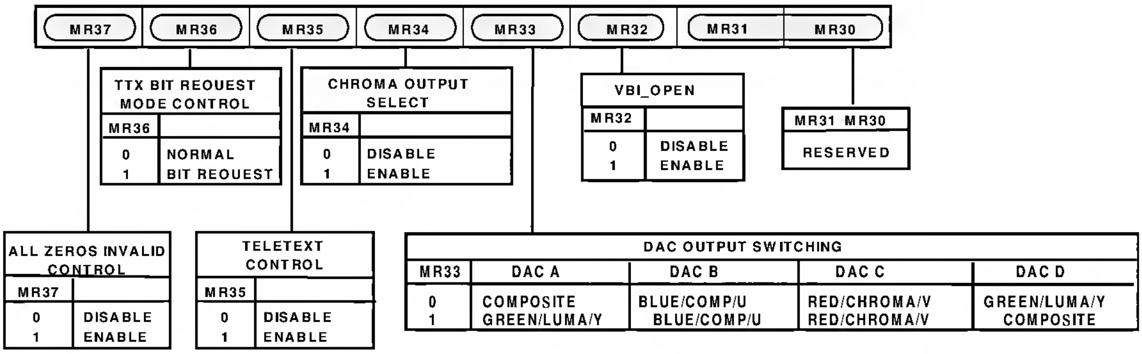


Figure 34 Mode Register 3

MODE REGISTER 4 MR4 (MR47-MR40)
(Address (SR4-SR0) = 04H)

Mode Register 4 is a 8-Bit wide register.
Figure 35 shows the various operations under the control of Mode Register 4.

-MR4 BIT DESCRIPTION-

Output Control (MR40):
This bit specifies if the part is in composite video or RGB/YUV mode. Note that in RGB/YUV mode the composite signal is still available.

RGB/YUV Control (MR41):
This bit enables the output from the RGB DACs to be set to YUV output video standard.

RGB Sync (MR42):
This bit is used to set up the RGB outputs with the sync information encoded on all RGB outputs.

VSYNC_3H Control (MR43):
When this bit is enabled ("1") in slave mode it is possible to drive the VSYNC active low input for 2.5 lines in PAL mode and 3 lines in NTSC mode.When this bit is enabled in master mode the ADV7170/ADV7171 outputs an active low VSYNC signal for 3 lines in NTSC mode and 2.5 lines in PAL mode.

Pedestal Control (MR44):
This bit specifies whether a pedestal is to be generated on the NTSC composite video signal.This bit is invalid if the ADV7170/ADV7171 is configured in PAL mode.

Active Video Filter Switching (MR45):
This bit, controls the filter mode applied outside the active video portion of the line. This filter ensures that the Sync rise and fall times are always on spec regardless of what Luma filter is selected. A logic "1" enables this mode.

Sleep Mode Control (MR46):
When this bit is set ("1") sleep mode is enabled. With this mode enabled the ADV7170/ADV7171 power consumption is reduced to typically 20μA. The I²C registers can be written to and read from when the ADV7170/ADV7171 is in Sleep Mode. If MR46 is set to a ("0") when the device is in Sleep Mode then the ADV7170/ADV7171 will come out of Sleep Mode and resume normal operation. Also if the RESET signal is applied during Sleep Mode the ADV7170/ADV7171 will come out of Sleep Mode and resume normal operation.

Reserved (MR47)
A logical 0 should be written to this bit

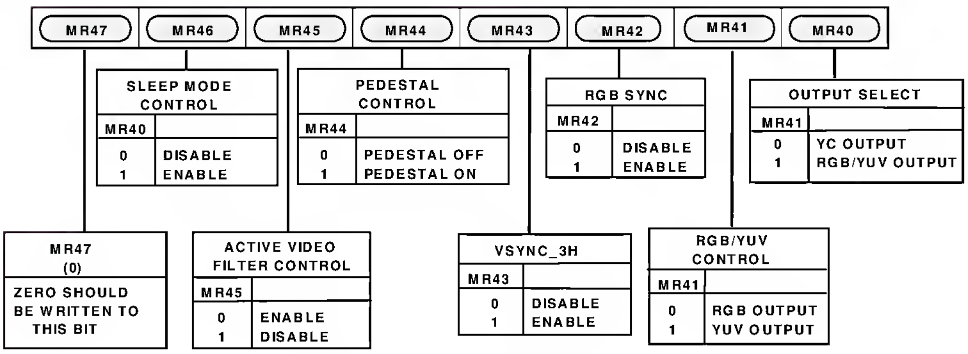


Figure 35. Mode Register 4

TIMING REGISTER 0 (TR07-TR00)
(Address (SR4-SR0) = 07H)

Figure 36 shows the various operations under the control of Timing Register 0. This register can be read from as well written to.

- TR0 BIT DESCRIPTION -

Master/Slave Control (TR00):
This bit controls whether the ADV7170/ADV7171 is in master or slave mode.

Timing Mode Control (TR02-TR01):
These bits control the timing mode of the ADV7170/ADV7171. These modes are described in the Timing and Control section of the datasheet.

$\overline{\text{BLANK}}$ Control (TR03):
This bit controls whether the $\overline{\text{BLANK}}$ input is used when the part is in slave mode.

Luma Delay Control (TR05-TR04):
These bits control the addition of a luminance delay. Each bit represents a delay of 74ns.

Pixel Port Select (TR06):
This bit is used to set the pixel port to accept 8-Bit or 16-Bit data. If an 8-Bit input is selected the data will be set up on pins P7-P0.

Timing Register Reset (TR07):
Toggling TR07 from low to high and low again resets the internal timing counters. This bit should be toggled after powerup, reset or changing to a new timing mode.

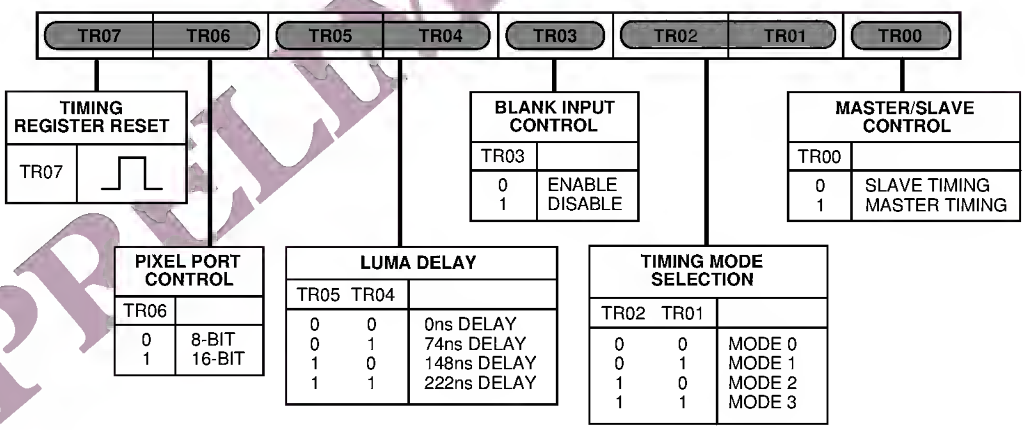


Figure 36. Timing Register 0

TIMING REGISTER 1 (TR17-TR10)
(Address (SR4-SR0) = 08H)

Timing Register 1 is a 8-Bit wide register.

Figure 37 shows the various operations under the control of Timing Register 1. This register can be read from as well written to. This register can be used to adjust the width and position of the master mode timing signals.

-TR1 BIT DESCRIPTION -

HSYNC Width (TR11-TR10):
These bits adjust the HSYNC pulse width.

HSYNC to VSYNC/FIELD Delay Control (TR13-TR12):
These bits adjust the position of the HSYNC output relative to the FIELD/VSYNC output.

HSYNC to FIELD Delay Control (TR15-TR14):
When the ADV7170/ADV7171 is in timing mode 1, these bits adjust the position of the HSYNC output relative to the FIELD output rising edge.

VSYNC Width (TR15-TR14):
When the ADV7170/ADV7171 is in timing mode 2, these bits adjust the VSYNC pulse width.

HSYNC to Pixel Data Adjust (TR17-TR16):
This enables the HSYNC to be adjusted with respect to the pixel data. This allows the Cr and Cb components to be swapped. This adjustment is available in both master and slave timing modes.

TR17	TR16	TR15	TR14	TR13	TR12	TR11	TR10

HSYNC TO PIXEL DATA ADJUSTMENT

TR17	TR16	
0	0	0 x T_{PCLK}
0	1	1 x T_{PCLK}
1	0	2 x T_{PCLK}
1	1	3 x T_{PCLK}

HSYNC TO FIELD RISING EDGE DELAY (MODE 1 ONLY)

TR15	TR14	T_c
x	0	T_b
x	1	T_b + 32μs

VSYNC WIDTH (MODE 2 ONLY)

TR15	TR14	
0	0	1 x T_{PCLK}
0	1	4 x T_{PCLK}
1	0	16 x T_{PCLK}
1	1	128 x T_{PCLK}

HSYNC TO FIELD/VSYNC DELAY

TR13	TR12	
0	0	0 x T_{PCLK}
0	1	4 x T_{PCLK}
1	0	16 x T_{PCLK}
1	1	64 x T_{PCLK}

HSYNC WIDTH

TR11	TR10	T_a
0	0	1 x T_{PCLK}
0	1	4 x T_{PCLK}
1	0	16 x T_{PCLK}
1	1	128 x T_{PCLK}

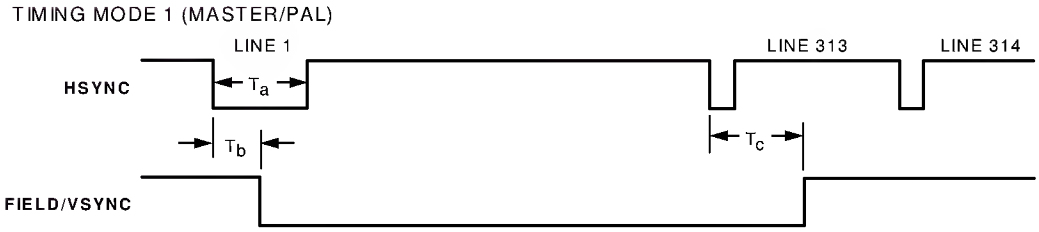


Figure 37. Timing Register 1

SUB-CARRIER FREQUENCY REGISTERS 3-0 (FSC3-FSC0)

(Address (SR4-SR0) = 09H-0CH)

These 8-Bit wide registers are used to set up the Sub-Carrier Frequency. The value of these registers are calculated by using the following equation:

$$\text{Sub-Carrier Frequency Register} = \frac{2^{32} - 1}{F_{CLK}} * F_{SCF}$$

i.e.: NTSC Mode,
F_{CLK} = 27 MHz,
F_{SCF} = 3.5795454 MHz

$$\text{Sub-Carrier Freq Value} = \frac{(2^{32}-1)}{27 \times 10^6} \text{ X } 3.5795454\text{x}10^6$$

$$= 21F07C16 \text{ HEX}$$

Figure 38 shows how the frequency is set up by the 4 registers

SUB-CARRIER PHASE REGISTER (FP7-FP0):
(Address (SR4-SR0) = 0DH)

This 8-Bit wide register is used to set up the Sub-Carrier Phase. Each bit represents 1.41°.

SUBCARRIER FREQUENCY REG 3	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
SUBCARRIER FREQUENCY REG 2	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
SUBCARRIER FREQUENCY REG 1	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC9	FSC8
SUBCARRIER FREQUENCY REG 0	FSC7	FSC6	FSC5	FSC4	FSC3	FSC2	FSC1	FSC0

Figure 38. Sub Carrier Frequency Register

CLOSED CAPTIONING EVEN FIELD DATA REGISTER 1-0 (CED15-CED00)

(Address (SR4-SR0) = 0E-0FH)

These 8-Bit wide registers are used to set up the closed captioning extended data bytes on Even Fields. Figure 39 shows how the high and low bytes are set up in the registers.

BYTE 1	CED15	CED14	CED13	CED12	CED11	CED10	CED9	CED8
BYTE 0	CED7	CED6	CED5	CED4	CED3	CED2	CED1	CED0

Figure 39. Closed Captioning Extended Data Register

CLOSED CAPTIONING ODD FIELD DATA REGISTER 1-0 (CCD15-CCD00)

(Subaddress (SR4-SR0) = 10-11H)

These 8-Bit wide registers are used to set up the closed captioning data bytes on Odd Fields. Figure 40 shows how the high and low bytes are set up in the registers.

BYTE 1	CCD15	CCD14	CCD13	CCD12	CCD11	CCD10	CCD9	CCD8
BYTE 0	CCD7	CCD6	CCD5	CCD4	CCD3	CCD2	CCD1	CCD0

Figure 40. Closed Captioning Data Register

NTSC PEDESTAL / PAL TELETEXT CONTROL REGISTERS 3-0 (PCE15-0, PCO15-0)/ (TXE15-0, TXO15-0)

(Subaddress (SR4-SR0) = 12-15H)

These 8-Bit wide registers are used to set up the NTSC pedestal/PAL Teletext on a line by line basis in the vertical blanking interval for both odd and even fields. Figure 41/42 shows the four control registers. A logic "1" in any of the bits of these registers has the effect of turning the Pedestal OFF on the equivalent line when used in NTSC. A logic "1" in any of the bits of these registers has the effect of turning Teletext ON on the equivalent line when used in PAL .

	LINE 17	LINE 16	LINE 15	LINE 14	LINE 13	LINE 12	LINE 11	LINE 10
FIELD 1/3	PCO7	PCO6	PCO5	PCO4	PCO3	PCO2	PCO1	PCO0
	LINE 25	LINE 24	LINE 23	LINE 22	LINE 21	LINE 20	LINE 19	LINE 18
FIELD 1/3	PCO15	PCO14	PCO13	PCO12	PCO11	PCO10	PCO9	PCO8
	LINE 280	LINE 279	LINE 278	LINE 277	LINE 276	LINE 275	LINE 274	LINE 273
FIELD 2/4	PCE7	PCE6	PCE5	PCE4	PCE3	PCE2	PCE1	PCE0
	LINE 288	LINE 287	LINE 286	LINE 285	LINE 284	LINE 283	LINE 282	LINE 281
FIELD 2/4	PCE15	PCE14	PCE13	PCE12	PCE11	PCE10	PCE9	PCE8

Figure 41. Pedestal Control Registers

	LINE 14	LINE 13	LINE 12	LINE 11	LINE 10	LINE 9	LINE 8	LINE 7
FIELD 1/3	TXO7	TXO6	TXO5	TXO4	TXO3	TXO2	TXO1	TXO0
	LINE 22	LINE 21	LINE 20	LINE 19	LINE 18	LINE 17	LINE 16	LINE 15
FIELD 1/3	TXO15	TXO14	TXO13	TXO12	TXO11	TXO10	TXO9	TXO8
	LINE 327	LINE 326	LINE 325	LINE 324	LINE 323	LINE 322	LINE 321	LINE 320
FIELD 2/4	TXE7	TXE6	TXE5	TXE4	TXE3	TXE2	TXE1	TXE0
	LINE 335	LINE 334	LINE 333	LINE 332	LINE 331	LINE 330	LINE 329	LINE 328
FIELD 2/4	TXE15	TXE14	TXE13	TXE12	TXE11	TXE10	TXE9	TXE8

Figure 42. Teletext Control Registers

TELETEXT CONTROL REGISTER TC07 (TC07-TC00)
(Address (SR4-SR0) = 19H)

Teletext Control Register is a 8-bit wide register.

TTXREQ Rising Edge Control (TC07-TC04) These bits control the position of the rising edge of TTXREQ. It can be programmed from zero CLOCK cycles to a max of 15 CLOCK cycles. See Figure 47.

TTXREQ Falling Edge Control (TC03-TC00)
These bits control the position of the falling edge of TTXREQ. It can be programmed from zero CLOCK cycles to a max of 15 CLOCK cycles. This controls the active window for Teletext data. Increasing this value reduces the amount of Teletext bits below the default of 360. If bits TC03-TC00 are unchanged when bits TC07-TC04 are changed then the falling egde of TTREQ will track that of the rising edge (i.e. the time between the falling and rising edge remains constant). See Figure 47.

TC07	TC06	TC05	TC04	TC03	TC02	TC01	TC00

TTXREQ Rising Edge Control				
TC07	TC06	TC05	TC04	
0	0	0	0	0 PCLK
0	0	0	1	1 PCLK
"	"	"	"	" PCLK
1	1	1	0	14 PCLK
1	1	1	1	15 PCLK

TTXREQ Falling Edge Control				
TC03	TC02	TC01	TC00	
0	0	0	0	0 PCLK
0	0	0	1	1 PCLK
"	"	"	"	" PCLK
1	1	1	0	14 PCLK
1	1	1	1	15 PCLK

Figure 43. Teletext Control Register

CGMS_WSS REGISTER 0 C/W0 (C/W07-C/W00)
(Address (SR4-SR0) = 16H)

CGMS_WSS register 0 is an 8-bit wide register.Figure 44 shows the operations under control of this register.

-C/W0 BIT DESCRIPTION-
CGMS Data Bits (C/W03-C/W00) :
These four data bits are the final four bits of CGMS data outputted.Note it is CGMS data ONLY in these bit positions i.e. WSS data does not share this location.

CGMS CRC Check Control (C/W04) :
When this bit is enabled ("1"), the last six bits of the CGMS data i.e. the CRC check sequence is calculated internally by the ADV7170/ADV7171. If this bit is disabled ("0") the values in the register are output.

CGMS Odd Field Control (C/W05) :
When this bit is set ("1") CGMS is enabled for odd fields.Note this is only valid in NTSC mode.

CGMS Even Field Control (C/W06) :
When this bit is set ("1") CGMS is enabled for even fields.Note this is only valid in NTSC mode.

WSS Control (C/W07) :
When this bit is set ("1"), wide screen signalling is enabled.Note this is only valid in PAL mode.

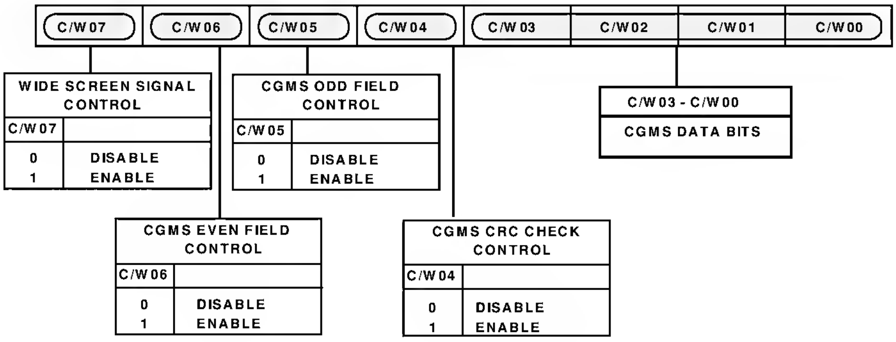


Figure 44. CGMS_WSS Register 0

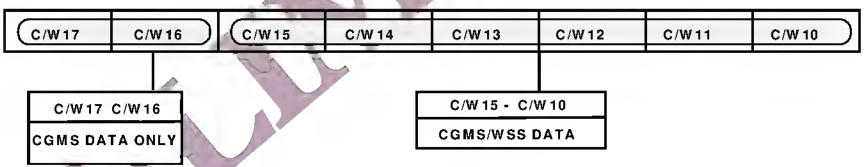
CGMS_WSS REGISTER 1 C/W1 (C/W17-C/W10) (Address (SR4-SR0) = 17H)
CGMS_WSS register 1 is an 8-bit wide register.Figure 45 shows the operations under control of this register.

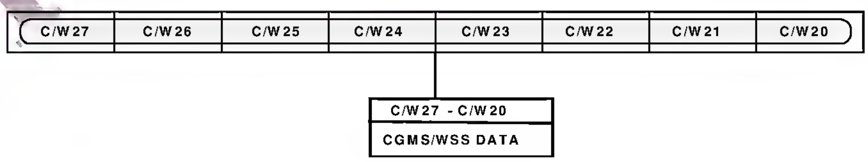
-C/W1 BIT DESCRIPTION-
CGMS/WSS Data Bits (C/W15-C/W10) :
These bit locations are shared by CGMS data and WSS data.In NTSC mode these bits are CGMS data.In PAL mode these bits are WSS data.

CGMS Data Bits (C/W17-C/W16) :
These bits are CGMS data bits only.

CGMS_WSS REGISTER 2 C/W1 (C/W27-C/W20) (Address (SR4-SR0) = 18H)
CGMS_WSS register 2 is an 8-bit wide register.Figure 46 shows the operations under control of this register.

-C/W2 BIT DESCRIPTION-
CGMS/WSS Data Bits (C/W27-C/W20) :
These bit locations are shared by CGMS data and WSS data.In NTSC mode these bits are CGMS data.In PAL mode these bits are WSS data.





APPENDIX 1

BOARD DESIGN AND LAYOUT CONSIDERATIONS

The ADV7170/ADV7171 is a highly integrated circuit containing both precision analog and high speed digital circuitry. It has been designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that these same design and layout techniques be applied to the system level design such that high speed, accurate performance is achieved. The "Recommended Analog Circuit Layout" shows the analog interface between the device and monitor.

The layout should be optimized for lowest noise on the ADV7170/ADV7171 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV7170/ADV7171 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7170/ADV7171, the analog output traces, and all the digital signal traces leading up to the ADV7170/ADV7171. The ground plane is the board's common ground plane.

Power Planes

The ADV7170/ADV7171 and any associated analog circuitry should have it's own power plane, referred to as the analog power plane (V_{AA}). This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7170/ADV7171.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7170/ADV7171 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with 0.1 µF ceramic capacitor decoupling. Each group of V_{AA} pins on the ADV7170/ADV7171 must have at least one 0.1 µF decoupling capacitor to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV7170/ADV7171 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the ADV7170/ADV7171 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7170/ADV7171 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The ADV7170/ADV7171 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

Digital Inputs, especially Pixel Data Inputs and clocking signals should never overlay any of the analog signal circuitry and should be kept as far away as possible.

For best performance, the outputs should each have a 75ohm load resistor connected to GND. These resistors should be placed as close as possible to the ADV7170/ADV7171 so as to minimize reflections.

The ADV7170/ADV7171 should have no inputs left floating. Any inputs that are not required should be tied to ground.

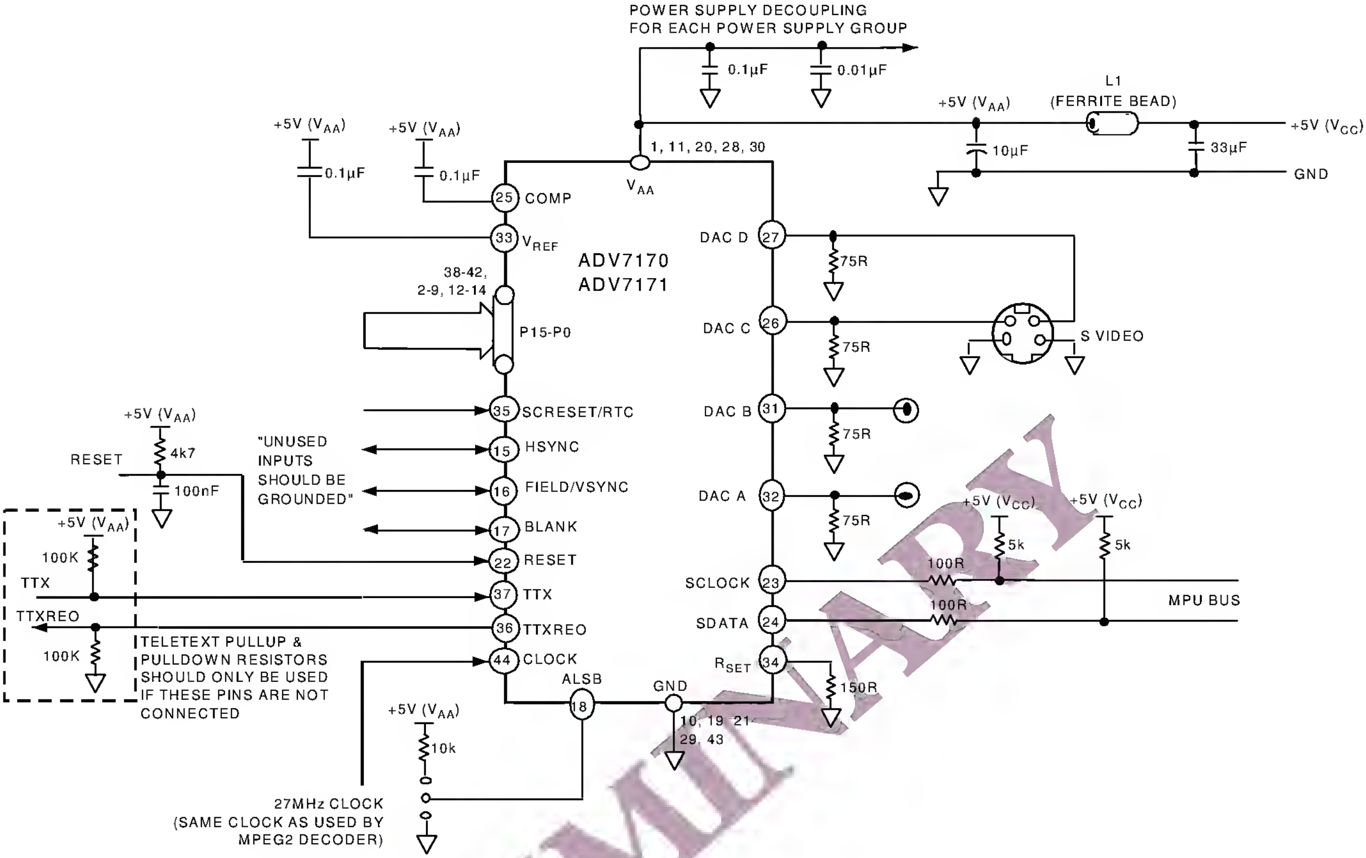


Figure 43 Recommended Analog Circuit Layout

The circuit below can be used to generate a 13.5 MHz waveform using the 27 MHz clock and the $\overline{\text{HSYNC}}$ pulse. This waveform is guaranteed to produce the 13.5 MHz clock in synchronization with the 27 MHz clock. This 13.5 MHz clock can be used if 13.5 MHz clock is required by the MPEG decoder. This will guarantee that the Cr and Cb pixel information is input to the ADV7170/ADV7171 in the correct sequence.

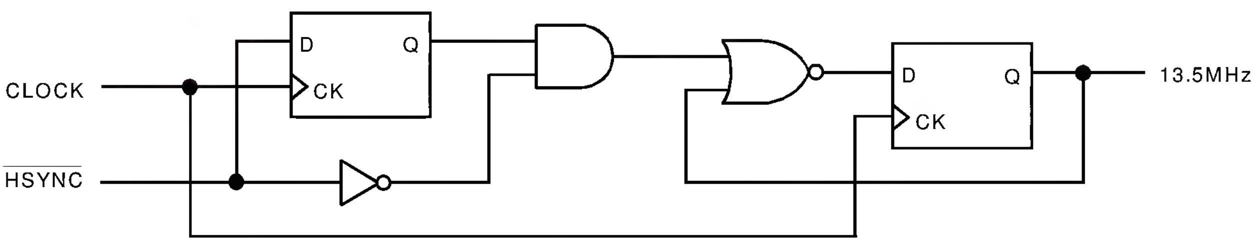


Figure 44 Circuit to generate 13.5 MHz

APPENDIX 2

CLOSED CAPTIONING

The ADV7170/ADV7171 supports closed captioning conforming to the standard Television Synchronizing Waveform for Color Transmission. Closed captioning is transmitted during the blanked active line time of line 21 of the odd fields and line 284 of even fields.

Closed captioning consists of a 7-cycle sinusoidal burst that is frequency and phase locked to the caption data. After the clock run in signal, the blanking level is held for two data bits and is followed by a logic level "1" start bit. 16 bits of data follow the start bit. These consist of two 8-bit bytes, seven data bits and one odd parity bit. The data for these bytes is stored in Closed Captioning Data Registers 0 and 1.

The ADV7170/ADV7171 also supports the extended closed captioning operation which is active during even fields and is encoded on scan line 284. The data for this operation is stored in Closed Captioning Extended Data Registers 0 and 1.

All clock run-in signals and timing to support Closed Captioning on lines 21 and 284 are generated automatically by the ADV7170/ADV7171. All pixels inputs are ignored during lines 21 and 284.

FCC Code of Federal Regulations (CFR) 47 section 15.119 and EIA608 describe the closed captioning information for lines 21 and 284.

The ADV7170/ADV7171 uses a single buffering method. This means that the Closed Captioning buffer is only one byte deep, therefore there will be no frame delay in outputting the Closed Captioning data unlike other two byte deep buffering systems. The data must be loaded one line before (line20 or line 283) it is outputted on line 21 and line 284. A typical implementation of this method is to uses VSYNC to interupt a microprocessor, which in turn will load the new data (two bytes) every field. If no new data is required for transmission you must insert zero's in both the data registers, this is called NULLING. It is also important to load 'control codes' all of which are double bytes on line 21 or a TV will not recognise them. If you have a message like "Hello World" which has an odd number of characters, it is important to pad it out to even inorder to get "end of caption" 2byte control code to land in the same field.

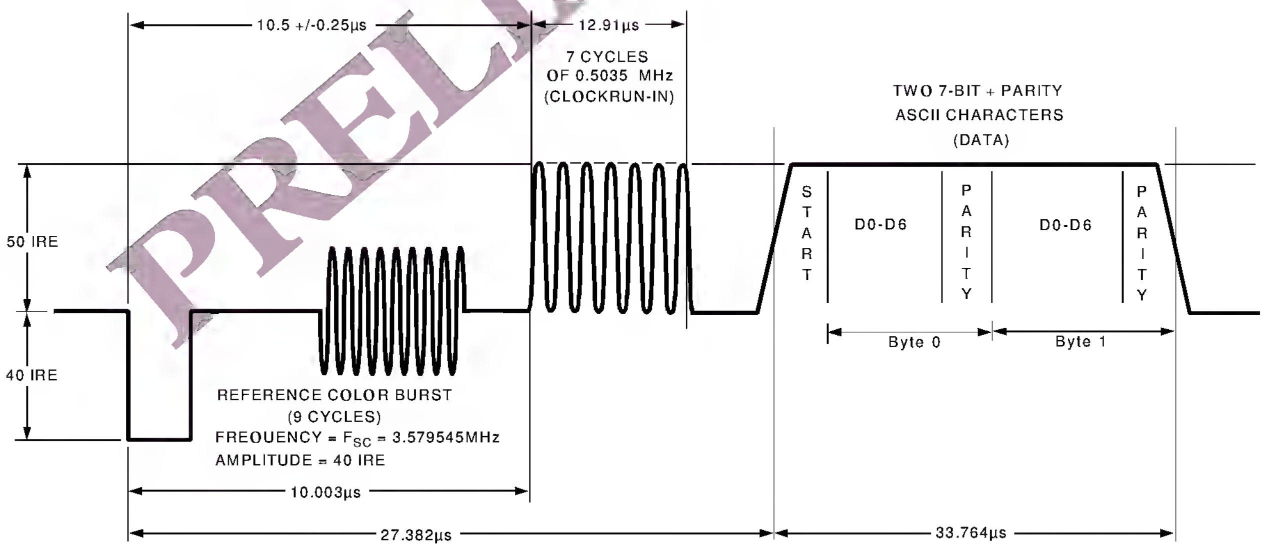


Figure 45 Closed Captioning Waveform (NTSC)

APPENDIX 3

COPY GENERATION MANAGEMENT SYSTEM (CGMS)

The ADV7170/ADV7171 supports Copy Generation Management System (CGMS) conforming to the standard. CGMS data is transmitted on line 20 of the odd fields and line 283 of even fields. Bits C/W05 and C/W06 control wheither or not CGMS data is output on ODD and EVEN fields. CGMS data can only be transmitted when the ADV7170/ADV7171 is configured in NTSC mode. The CGMS data is 20 bits long, the function of each of these bits is as shown below. The CGMS data is preceeded by a reference pulse of the same amplitudeand duration as a CGMS bit, see figure below. The bits are output from the configuration registers in the following order; C/W00 = C16, C/W01= C17, C/W02 = C18, C/W03 = C19, C/W10 = C8 , C/W11 = C9, C/W12 = C10, C/W13 = C11, C/W14 = C12, C/W15 = C13, C/W16 = C14 , C/W17 = C15 , C/W20 = C0 , C/W21 = C1, C/W22 = C2, C/W23 = C3, C/W24 = C4, C/W25 = C5, C/W26 = C6, C/W27= C7. If the bit C/W04 is set to a logic "1", the last six bits C19-C14 which comprise the 6-bit CRC check sequence are calculated automatically on the ADV7170/ADV7171 based on the lower 14 bits (C0-C13) of the data in the data registers and output with the remaing 14-bits to form the complete 20-bits of the CGMS data. The calculation of the CRC sequence is based on the ploynomial $X^6 + X + 1$ with a preset value of 111111. If C/W04 is set to a logic "0" then all 20-bits (C0-C19) are output directly from the CGMS registers (no CRC calculated, must be calculated by the user).

Function of CGMS bits:

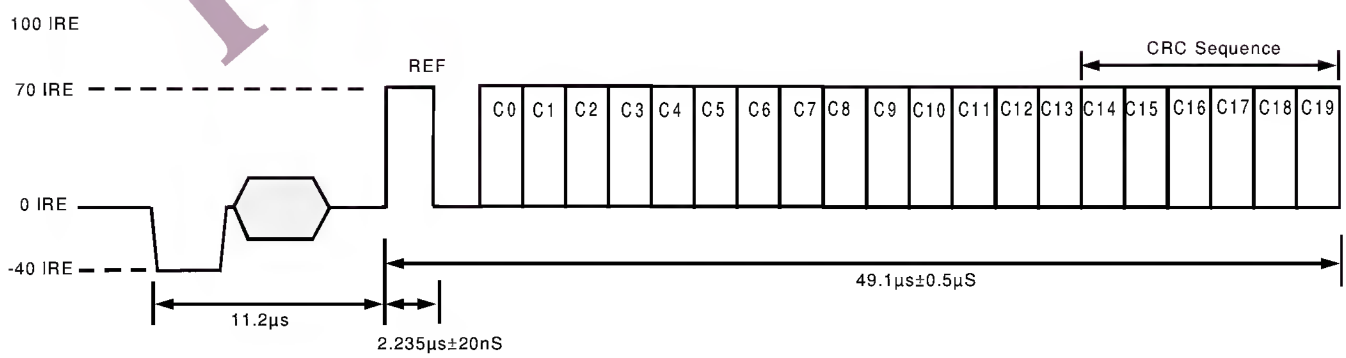
WORD 0 - 6 BITS
WORD 1 - 4 BITS
WORD 2 - 6 BITS
CRC - 6 BITS CRC polynomial = $X^6 + X + 1$ (preset to 111111)

WORD 0		1	0
B1	Aspect ratio	16:9	4:3
B2	Display format	Letterbox	Normal
b3	Undefined		

WORD 0
B4,B5,B6 Identification information about video and other signals (e.g. audio)

WORD 1
B7,B8,B9,B10 Identification signal incidental to word 0

WORD 2
B11,B12,B13,B14 Identification signal and information incidental to word 0



CGMS Waveform diagram

APPENDIX 4

WIDE SCRENN SIGNALLING

The ADV7170/ADV7171 supports Wide Screen Signalling (WSS) conforming to the standard. WSS data is transmitted on line 23. WSS data can only be transmitted when the ADV7170/ADV7171 is configured in PAL mode. The WSS data is 14-bits long, the function of each of these bits is as shown below. The WSS data is preceeded by a run-in sequence and a Start Code, see figure below. The bits are output from the configuration registers in the following order; C/W20 = W0, C/W21= W1, C/W22 = W2, C/W23 = W3, C/W24 = W4 , C/W25 = W5, C/W26 = W6, C/W27 = W7, C/W10 = W8, C/W11 = W9, C/W12 = W10 , C/W13 = W11 , C/W14 = W12 , C/W15 = W13 . If the bit C/W07 is set to a logic "1" it enables the WSS data to transmitted on line 23. The latter portion of line 23 (42.5μSfrom the falling edge of Hsync) is available for the insertion of video.

Function of CGMS bits:

bit 0 - bit 2 Aspect Ratio / Format / Position
bit 3 is odd parity check of bit 0 - bit 2

b0, b1, b2, b3	Aspect Ratio	Format	Position
0 0 0 1	4:3	full format	non-applicable
1 0 0 0	14:9	letterbox	centre
0 1 0 0	14:9	letterbox	top
1 1 0 1	16:9	letterbox	centre
0 0 1 0	16:9	letterbox	top
1 0 1 1	>16:9	letterbox	centre
0 1 1 1	14:9	full format	centre
1 1 1 0	16:9	non-applicable	non-applicable

b4
0 Camera mode
1 Film mode

b5
0 Standard coding
1 Motion Adaptive Colour Plus

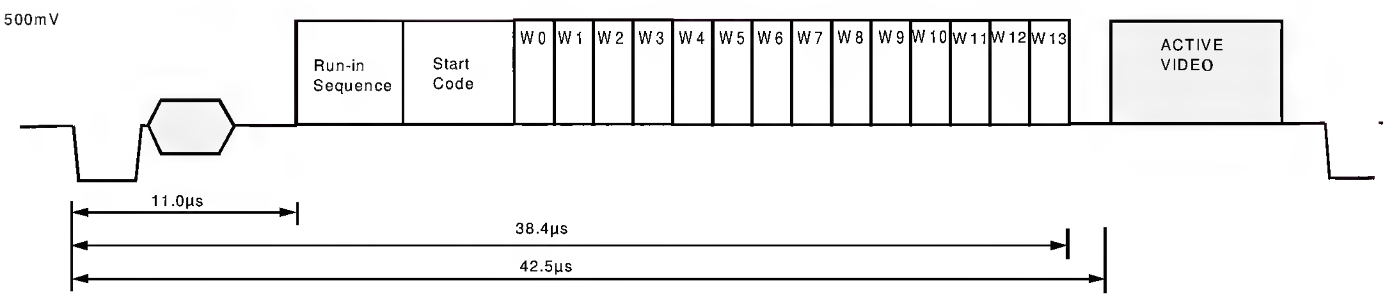
b6
0 No Helper
1 Modulated Helper

b7 RESERVED

b9 b10
0 0 No open subtitles
1 0 Subtitles in active image area
0 1 Subtitles out of active image area
1 1 Reserved

b11
0 No surround sound information
1 Surround sound mode

b12 RESERVED
b13 RESERVED



WSS Waveform diagram

APPENDIX 5

Teletext Insertion

Time T_{PD} time needed by the ADV7170/71 to interpolate input data on TTX and insert it onto the CVBS or Y outputs, such that it appears $T_{synTxtOut}$ = 10.2uS after the leading edge of the horizontal signal. Time Txt_{Del} is the pipeline delay time by the source that is gated by the TTREQ signal order to deliver TTX data.
With the programability that is offered with TTXREQ signal on the Rising/Falling edges, the TTX data is always inserted at the correct position of 10.2us after the leading edge of Horizontal Sync pulse, thus this enables a source interface with variable pipeline delays.
The width of the TTXREQ signal must always be maintained such that it allows the insertion of 360 (inorder to comply with the Teletext Standard "PAL-WST") teletext bits at a text data rate of 6.9375Mbits/s, this is acheived by setting TC03-TC00 to zero. The insertion window is not open if the Teletex Enable bit (MR34) is set to zero.

Teletext Protocol

The relationship between the TTX bit clock (6.9375MHz) and the system CLOCK (27MHz) for 50Hz is given as follows:

$(27Mhz / 4) = 6.75MHz$
$(6.9375 \times 10^6 / 6.75 \times 10^6 = 1.027777$

Thus 37 TTX bits correspond to 144 clocks (27MHz), each bit has a width of almost 4 clock cycles. The ADV7170/76A uses an internal sequencer and variable phase interpolation filter to minimise the phase jitter and thus generate a bandlimited signal which can be outputed on the CVBS and Y outputs.

At the TTX input the bit duration scheme repeats after every 37 TTX bits or 144 clock cycles. The protocol requires that TTX bits 10, 19, 28, 37 are carried by three clock cycles, all other bits by four clock cycles. After 37 TTX bits, the next bits with three clock cycles are 47, 56, 65 and 74. This scheme holds for all following cycles of 37 TTX bits, until all 360 TTX bits are completed. All teletext lines are implemented in the say way. Individual control of teletext lines are controlled by Teletext Setup Registers.

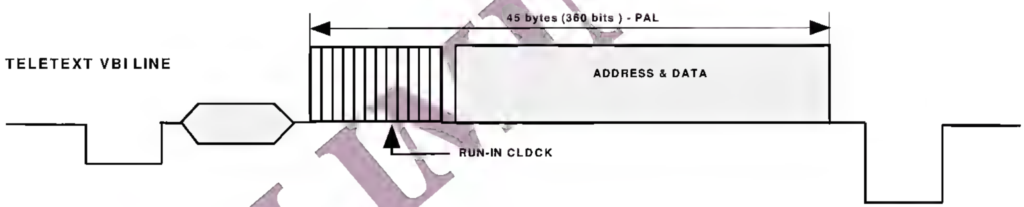
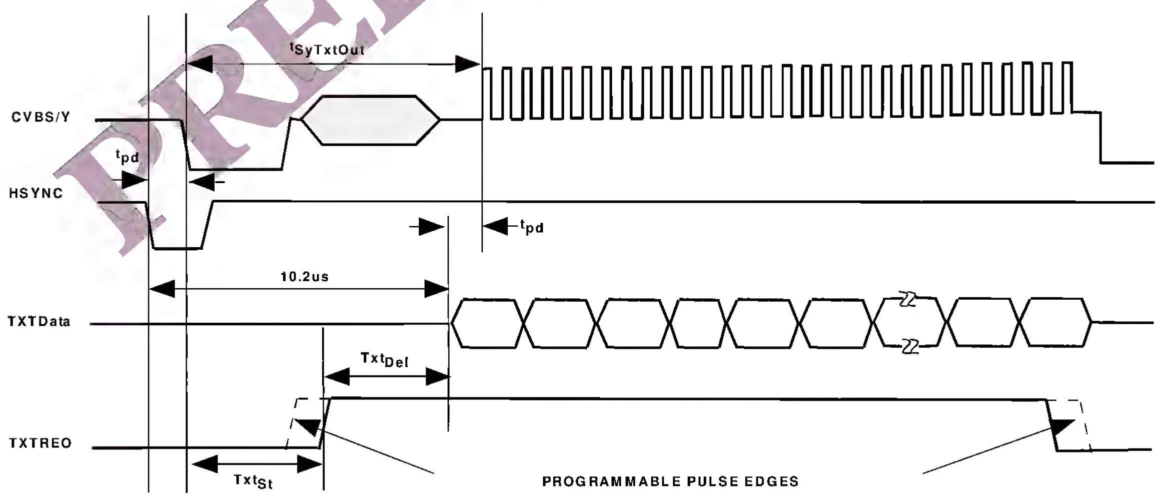


Figure 46 Teletext VBI Line



$T_{synTxtOut}$ = 10.2us .
T_{pd} = PipeLine Delay Through ADV7170/76A.
Txt_{Del} = TTXREQ to TTX (Programmable Range = 4-bits [0-15 clock cycles]).

Figure 47 Teltext Functionality Diagram

APPENDIX 6

NTSC WAVEFORMS (WITH PEDESTAL)

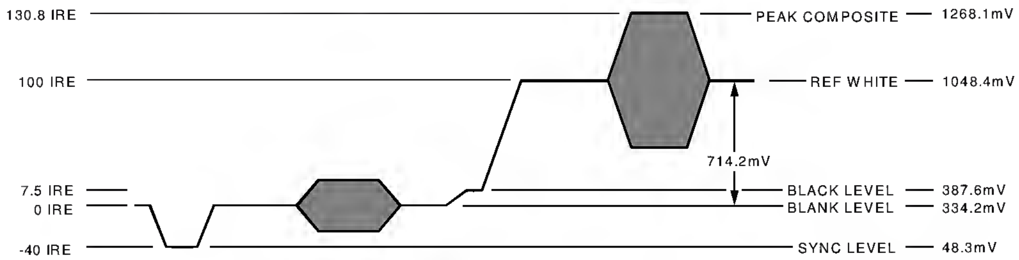


Figure 48 NTSC Composite Video Levels

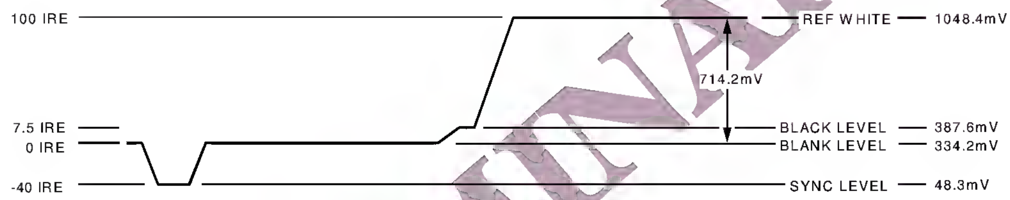


Figure 49 NTSC Luma Video Levels

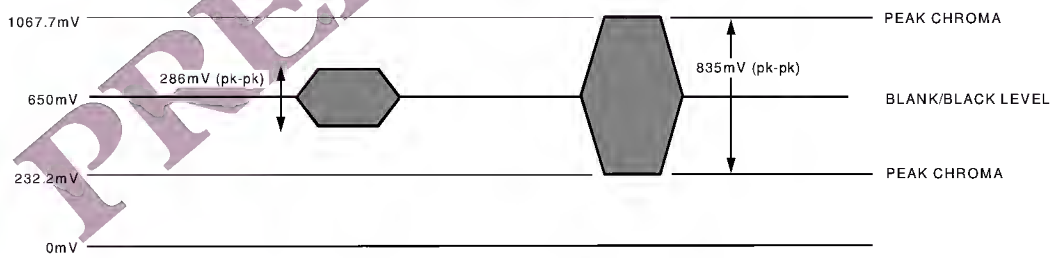


Figure 50 NTSC Chroma Video Levels

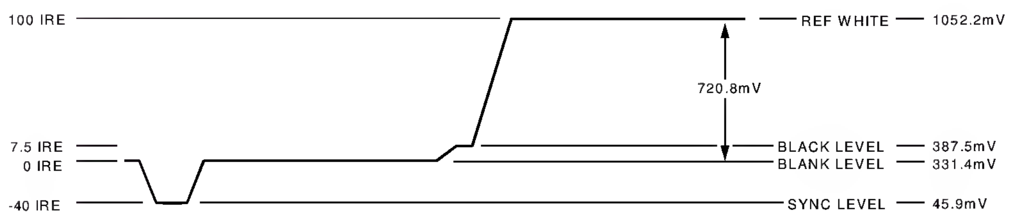


Figure 51 NTSC RGB Video Levels

NTSC WAVEFORMS (WITHOUT PEDESTAL)

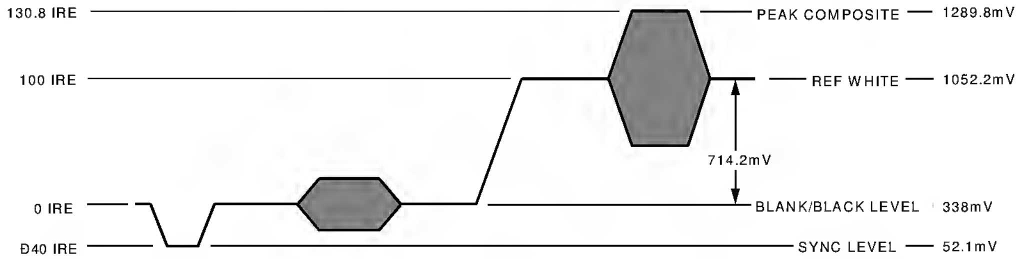


Figure 52 NTSC Composite Video Levels

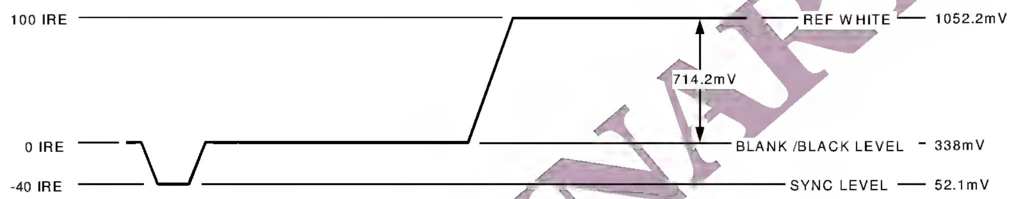


Figure 53 NTSC Luma Video Levels

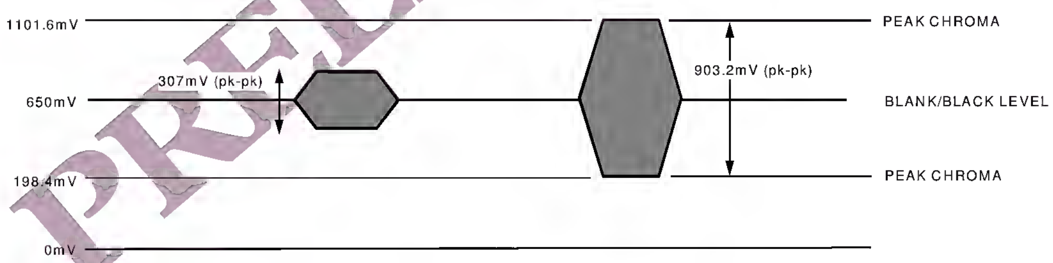


Figure 54 NTSC Chroma Video Levels

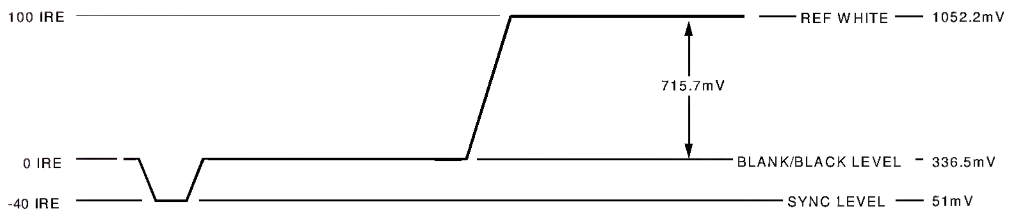


Figure 55 NTSC RGB Video Levels

PAL WAVEFORMS

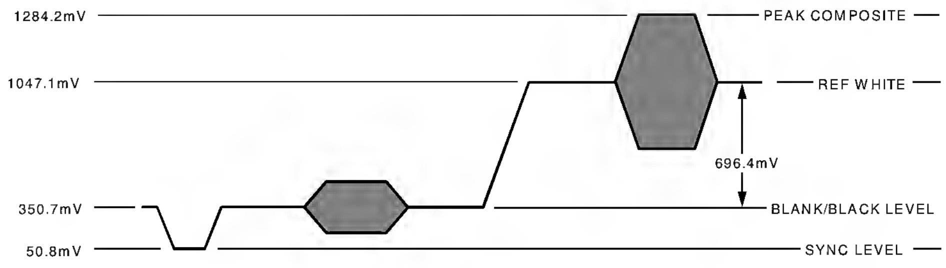


Figure 56 PAL Composite Video Levels

Figure 57 PAL Luma Video Levels

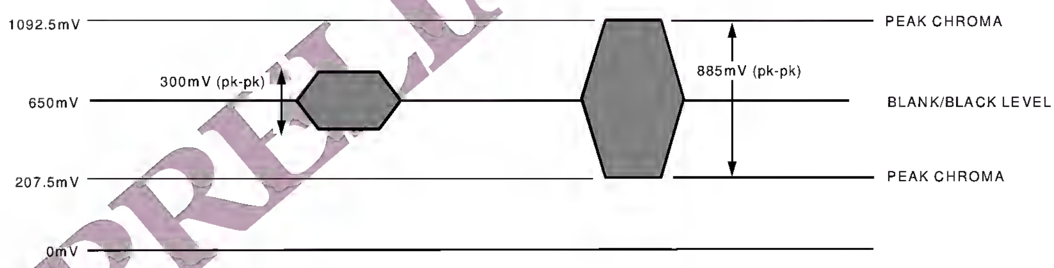


Figure 58 PAL Chroma Video Levels

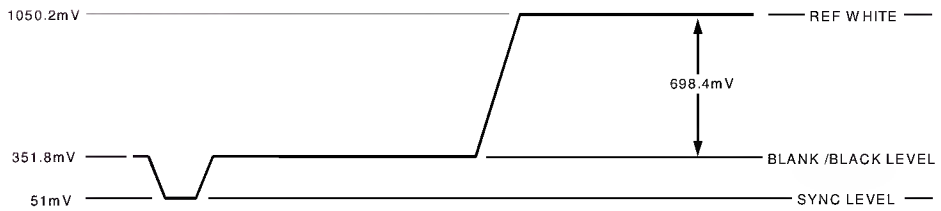


Figure 59 PAL RGB Video Levels

UV WAVEFROMS

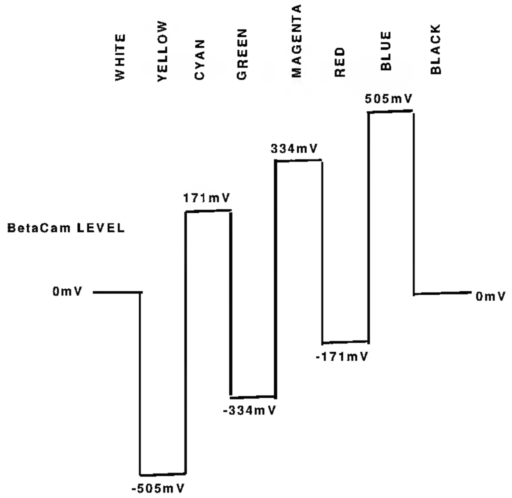


Figure 60 NTSC 100% Color Bars No Pedestal U Levels

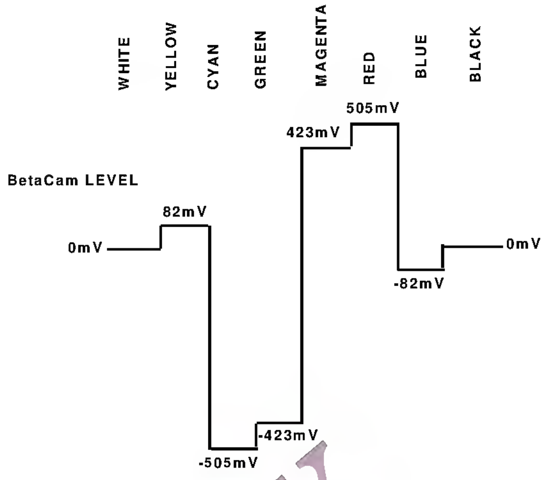


Figure 61 NTSC 100% Color Bars No Pedestal V Levels

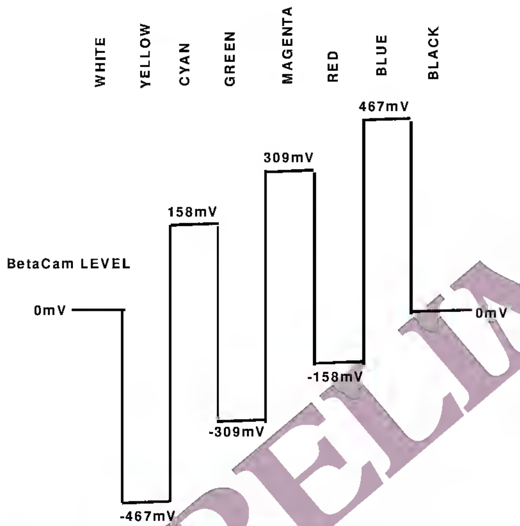


Figure 62 NTSC 100% Color Bars with Pedestal U Levels

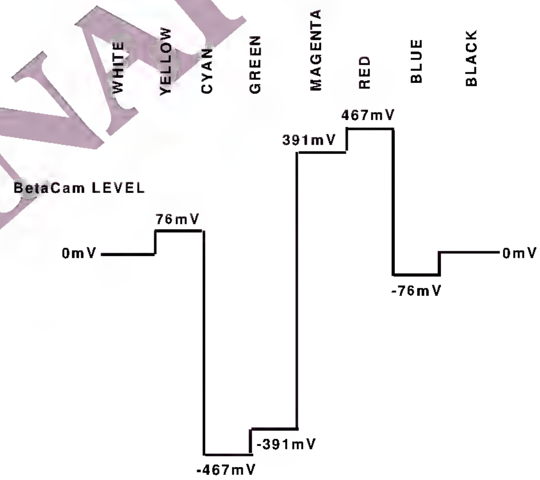


Figure 63 NTSC 100% Color Bars with Pedestal V Levels

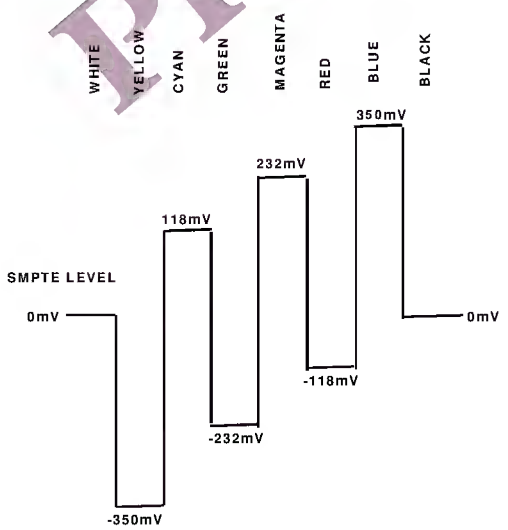


Figure 64 PAL 100% Color Bars U Levels

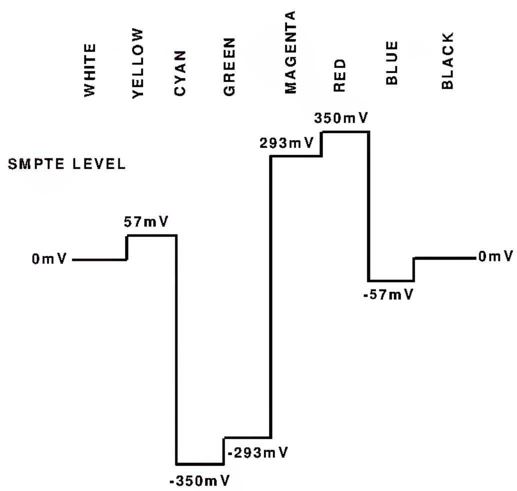


Figure 65 PAL 100% Color Bars V Levels

APPENDIX 7

DAC BUFFERING

Whwn External Buffering is needed of the ADV7170/71 DAC outputs, the configuration in Figure 70 is recommended. This configuration shows the DAC outputs runing at half(18mA) their full current(36mA) capability. This will allow the ADV7170/76A to dissapate less power, the analog current is reduced by 50% with a Rset of 300ohms and a Rload of 75ohms. This mode is recommended for 3.3volt operation as optimum performance is obtained from the DAC outputs at 18mA with a V_{AA} of 3.3volts. This buffer also adds extra isolation on the video outputs, see buffer circuit in Figure 71. When calculating Absolute Output Full Scale Current and Voltage use the following equations:

$\mathbf{V_{OUT} = I_{OUT} * R_{LOAD}}$

$\mathbf{I_{OUT} = (V_{REF} * K) / R_{SET}}$ **K= 4.2146 constant, $\mathbf{V_{REF} = 1.235V}$**

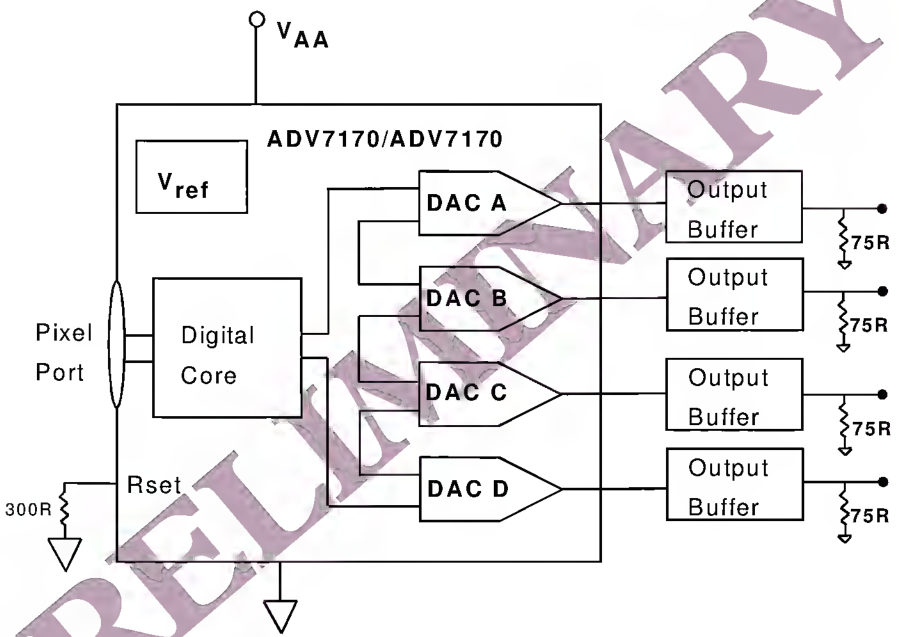


Figure 70 Output DAC Buffering Configuration

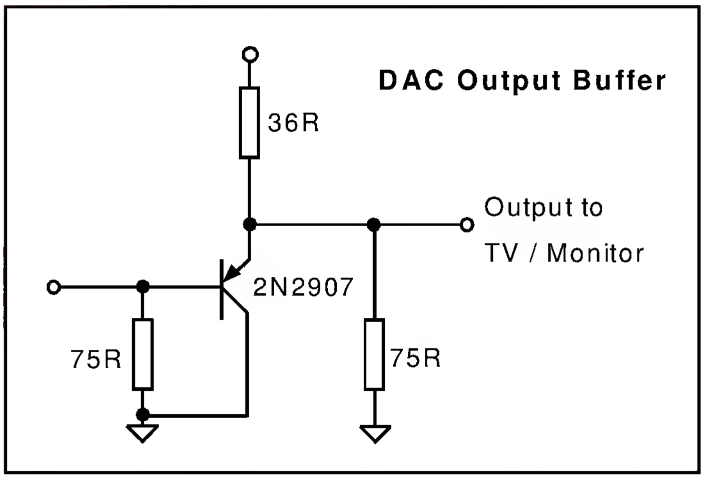


Figure 71 Recommended Output DAC Buffer

APPENDIX 8

OUTPUT FILTER

If an output filter is required for the CVBS, Y, UV, Chroma and RGB outputs of the ADV7170/ADV7171, the following filter in Figure 66 can be used. Plots of the filter characteristics are shown in Figure 67, Figure 68 and Figure 69. An Output Filter is not required if the Outputs of the ADV7170/ADV7171 are connected to most analog monitors or TVs, however if the Output signals are applied to a system where sampling is used (eg. Digital TVs) then a filter is required to prevent alaising.

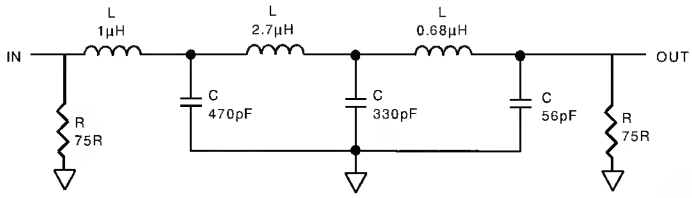


Figure 66 Output Filter

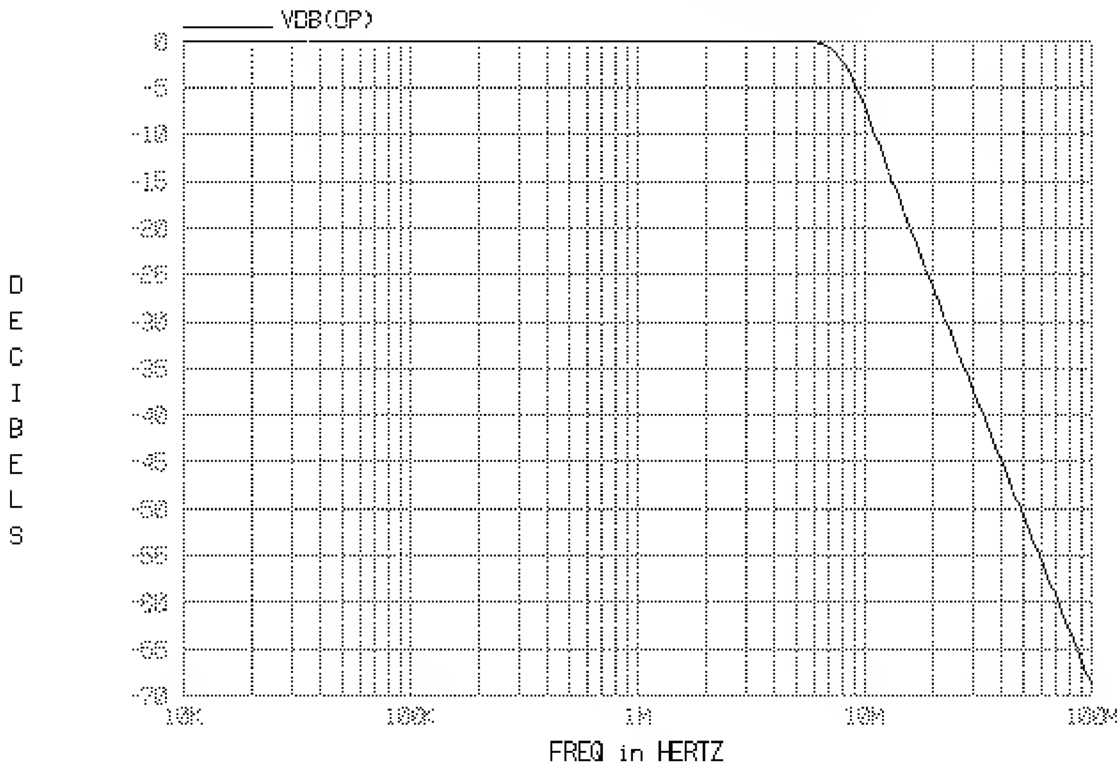


Figure 67 Output Filter Plot

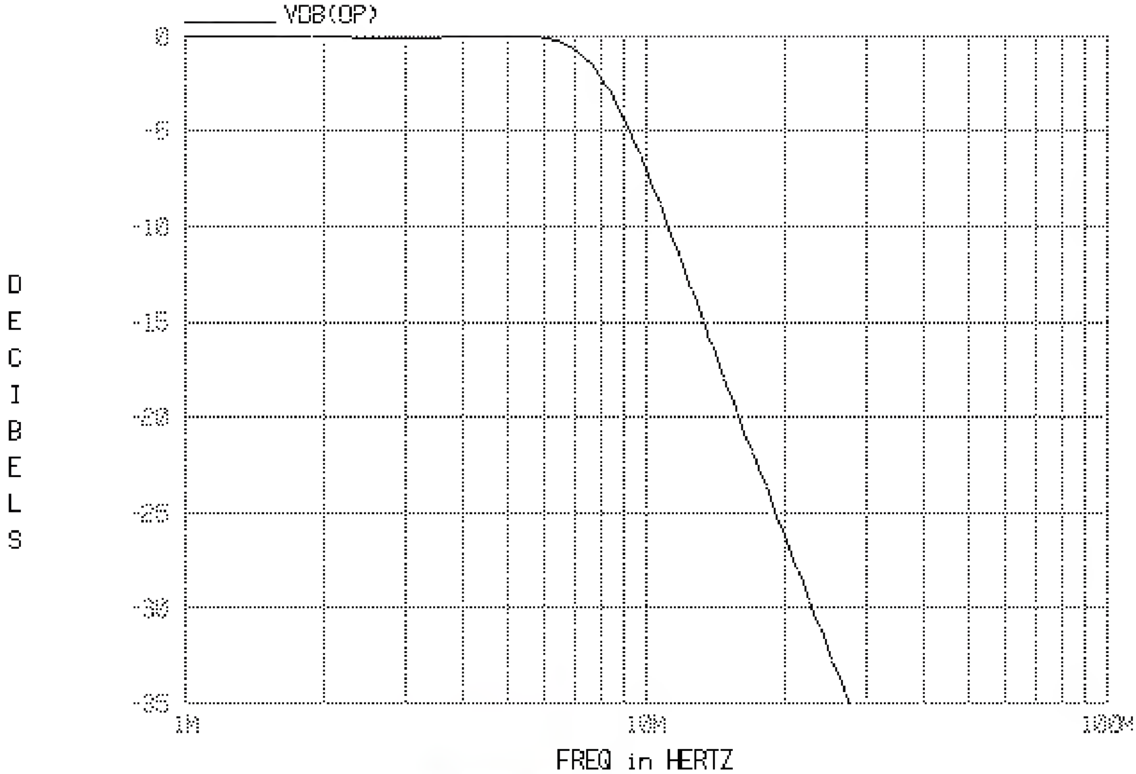


Figure 68 Output Filter Close up

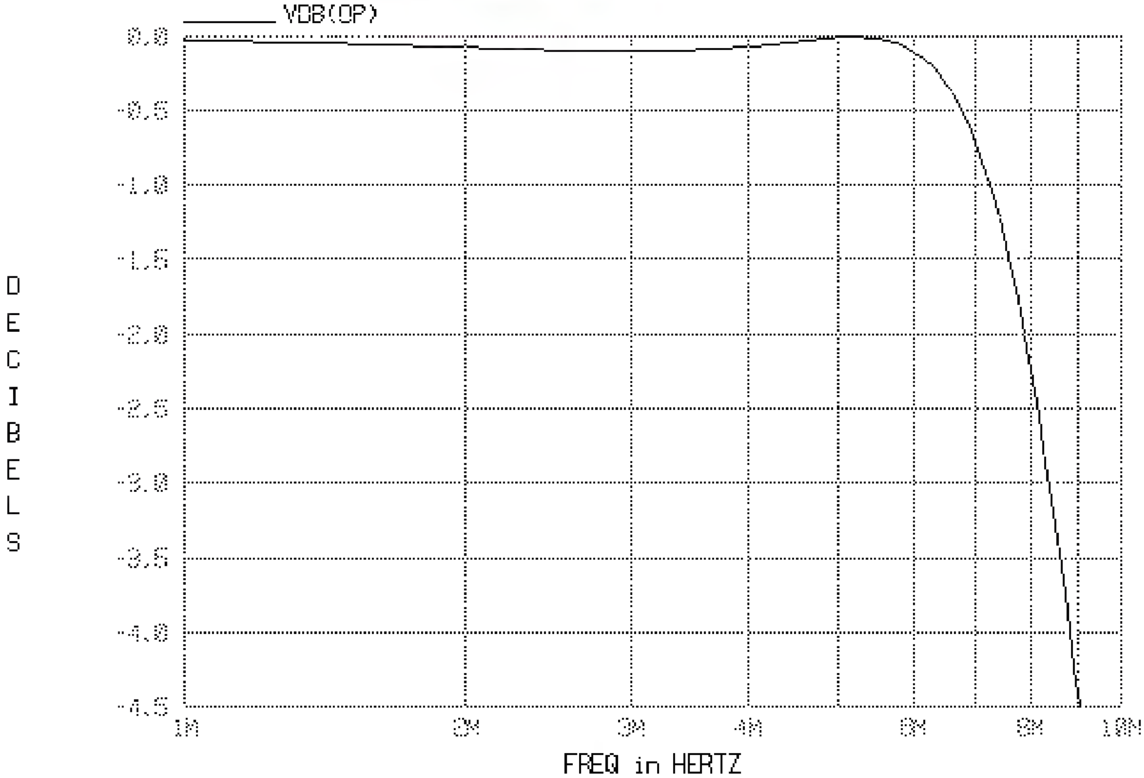


Figure 69 Output Filter Plot Close up